N and P-Channel 60V (D-S) Power MOSFET

FEATURES

- Low gate charge for fast power switching
- 100% UIS and R_g tested
- RoHS Compliant
- Halogen-free

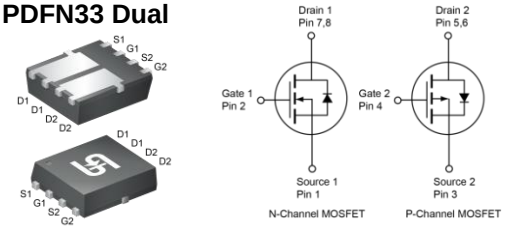
APPLICATIONS

- BLDC Fan
- Motor Drives

KEY PERFORMANCE PARAMETERS				
PARAMETER		**TYPE**	**VALUE**	**UNIT**
V_{DS}		N-ch	60	V
		P-ch	-60	
$R_{DS(on)}$ (max)	V_{GS} = 10V	N-ch	98	mΩ
	V_{GS} = 4.5V		137	
	V_{GS} = -10V	P-ch	168	
	V_{GS} = -4.5V		235	
Q_g		N-ch	9.6	nC
		P-ch	8.6	

Pb-Free RoHS COMPLIANT HALOGEN FREE

PDFN33 Dual



Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)					
PARAMETER		**SYMBOL**	**N-ch**	**P-ch**	**UNIT**
Drain-Source Voltage		V_{DS}	60	-60	V
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current, Silicon limited	T_C = 25°C	I_D	8.2	-6.6	A
Continuous Drain Current (Note 1)	T_C = 25°C	I_D	5.7	-4.5	A
	T_A = 25°C		2.7	-2.2	
Pulsed Drain Current (Note 2)		I_{DM}	22.8	-18	A
Single Pulse Avalanche Current (Note 3)		I_{AS}	6.5	-7.4	A
Single Pulse Avalanche Energy (Note 3)		E_{AS}	6.4	8.3	mJ
Total Power Dissipation	T_C = 25°C	P_D	14	14	W
	T_C = 125°C		2.7	2.7	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150		°C

THERMAL PERFORMANCE			
PARAMETER	**SYMBOL**	**MAXIMUM**	**UNIT**
Thermal Resistance – Junction to Case	$R_{\Theta JC}$	9.2	°C/W
Thermal Resistance – Junction to Ambient (Note 4)	$R_{\Theta JA}$	81	

NOTE:

1. Package current limit.
2. Pulse Width ≤ 100μs.
3. L = 0.3mH, VGS = 10V, RG = 25Ω, Starting TJ = 25°C.
4. Device on a PCB FR4 with 1 in^2 (single layer, 2 oz thick) copper area for drain connection.

ELECTRICAL SPECIFICATIONS (T_A = 25°C unless otherwise noted)							
PARAMETER	**CONDITIONS**	**SYMBOL**	**TYPE**	**MIN**	**TYP**	**MAX**	**UNIT**
Static							
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	BV_{DSS}	N-ch	60	--	--	V
	V_{GS} = 0V, I_D = -250μA		P-ch	-60	--	--	
Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	$V_{GS(TH)}$	N-ch	1.2	1.7	2.5	V
	V_{GS} = V_{DS}, I_D = -250μA		P-ch	-1	-1.5	-2.5	
Gate-Source Leakage Current	V_{GS} = ±20V, V_{DS} = 0V	I_{GSS}	N-ch	--	--	±100	nA
	V_{GS} = ±20V, V_{DS} = 0V		P-ch	--	--	±100	nA
Drain-Source Leakage Current	V_{GS} = 0V, V_{DS} = 60V	I_{DSS}	N-ch	--	--	1000	nA
	V_{GS} = 0V, V_{DS} = -60V		P-ch	--	--	-1000	
Drain-Source On-State Resistance (Note 5)	V_{GS} = 10V, I_D = 2.8A	$R_{DS(on)}$	N-ch	--	75	98	mΩ
	V_{GS} = 4.5V, I_D = 2.8A			--	85	137	
	V_{GS} = -10V, I_D = -2.2A		P-ch	--	129	168	
	V_{GS} = -4.5V, I_D = -2.2A			--	161	235	
Forward Transconductance (Note 5)	V_{DS} = 10V, I_D = 0.7A	g_{fs}	N-ch	--	5.2	--	S
	V_{DS} = -10V, I_D = -0.6A		P-ch	--	3.1	--	
Dynamic (Note 6)							
Total Gate Charge	N-ch V_{DS} = 30V, I_D = 2.7A V_{GS} = 10V P-ch V_{DS} = -30V, I_D = -2.2A V_{GS} = -10V	Q_g	N-ch	--	9.6	--	nC
			P-ch	--	8.6	--	
Gate-Source Charge		Q_{gs}	N-ch	--	1.8	--	
			P-ch	--	1.3	--	
Gate-Drain Charge		Q_{gd}	N-ch	--	1.4	--	
			P-ch	--	1.7	--	
Input Capacitance	N-ch V_{GS} = 0V, V_{DS} = 30V f = 1.0MHz P-ch V_{GS} = 0V, V_{DS} = -30V f = 1.0MHz	C_{iss}	N-ch	--	527	--	pF
			P-ch	--	425	--	
Output Capacitance		C_{oss}	N-ch	--	27	--	
			P-ch	--	30	--	
Reverse Transfer Capacitance		C_{rss}	N-ch	--	22	--	
			P-ch	--	26	--	
Gate Resistance	f = 1.0MHz	R_g	N-ch	--	1.3	--	Ω
			P-ch	--	15	--	

Notes:

5. Pulse test: Pulse Width ≤ 300μs, duty cycle ≤ 2%.
6. Defined by design. Not subject to production test.

ELECTRICAL SPECIFICATIONS (T_A = 25°C unless otherwise noted)							
PARAMETER	**CONDITIONS**	**SYMBOL**	**TYPE**	**MIN**	**TYP**	**MAX**	**UNIT**
Switching (Note 7)							
Turn-On Delay Time	N-ch V_{GS} = 10V, V_{DS} = 30V, I_D = 2.7A, R_G = 3.3Ω P-ch V_{GS} = -10V, V_{DS} = -30V, I_D = -2.2A, R_G = 3.3Ω	$t_{d(on)}$	N-ch	--	5.8	--	ns
			P-ch	--	5.1	--	
Turn-On Rise Time		t_r	N-ch	--	12	--	
			P-ch	--	8.2	--	
Turn-Off Delay Time		$t_{d(off)}$	N-ch	--	14	--	
			P-ch	--	20	--	
Turn-Off Fall Time		t_f	N-ch	--	1.8	--	
			P-ch	--	17	--	
Source-Drain Diode							
Forward Voltage (Note 5)	V_{GS} = 0V, I_S = 2.8A	V_{SD}	N-ch	--	--	1	V
	V_{GS} = 0V, I_S = -2.2A		P-ch	--	--	-1	
Reverse Recovery Time	N-ch I_S = 2.7A, dI/dt = 100A/μs P-ch I_S = -2.2A, dI/dt = 100A/μs	t_{rr}	N-ch	--	12	--	ns
			P-ch	--	9.5	--	
Reverse Recovery Charge		Q_{rr}	N-ch	--	7.8	--	nC
			P-ch	--	5.1	--	

Notes:
7. Switching time is essentially independent of operating temperature.

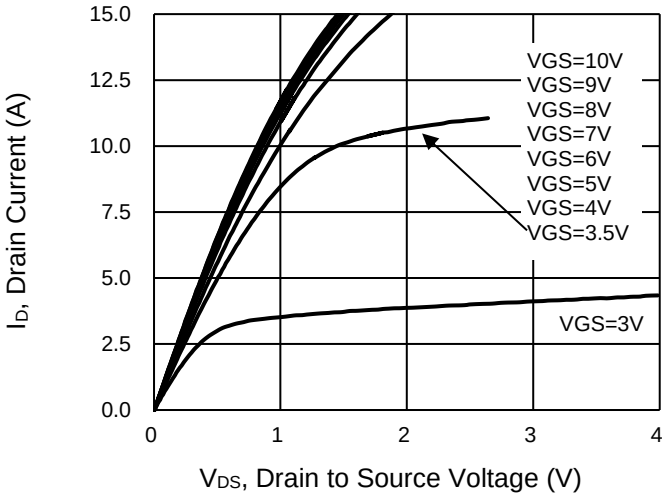
ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TSM8588CV RGG	PDFN33 Dual	5,000pcs / 13” Reel

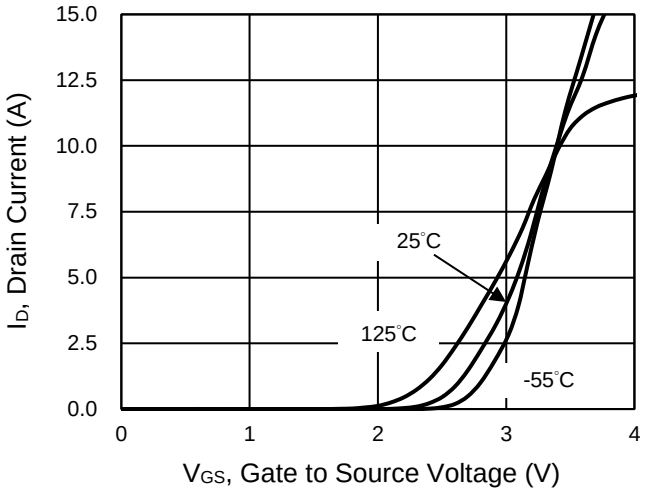
CHARACTERISTICS CURVES (N-Channel)

(T_A = 25°C unless otherwise noted)

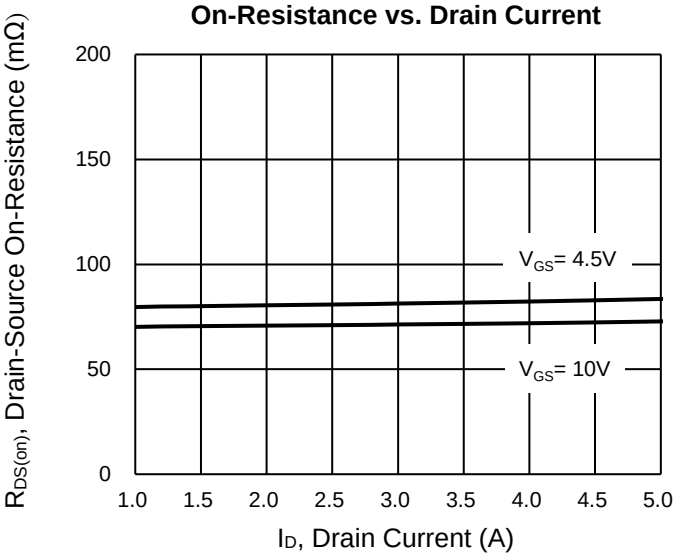
Output Characteristics



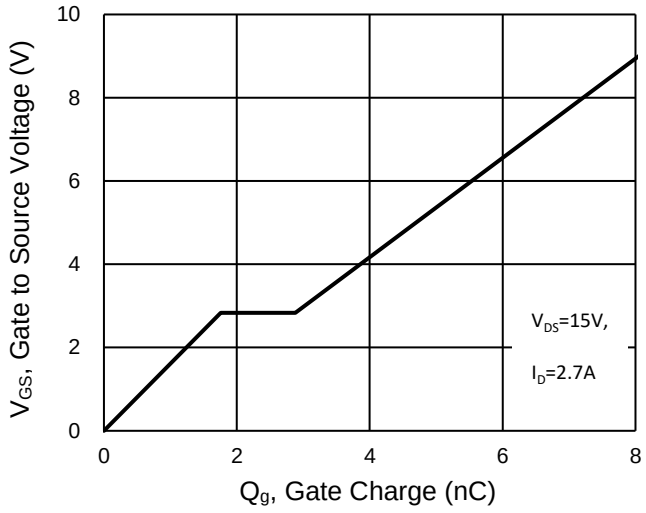
Transfer Characteristics



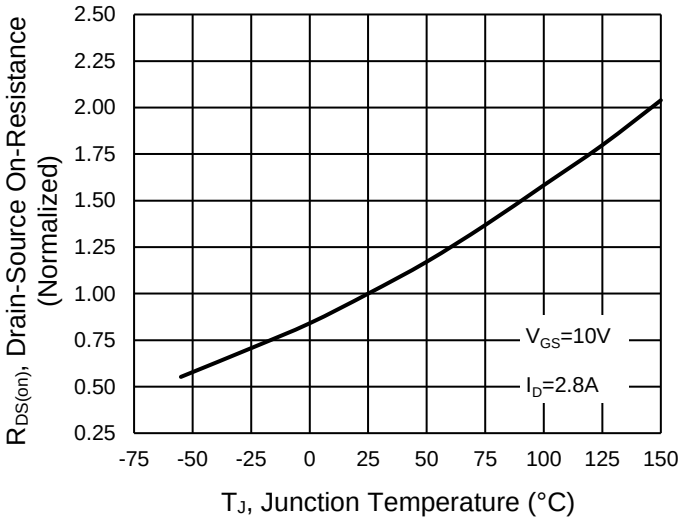
On-Resistance vs. Drain Current



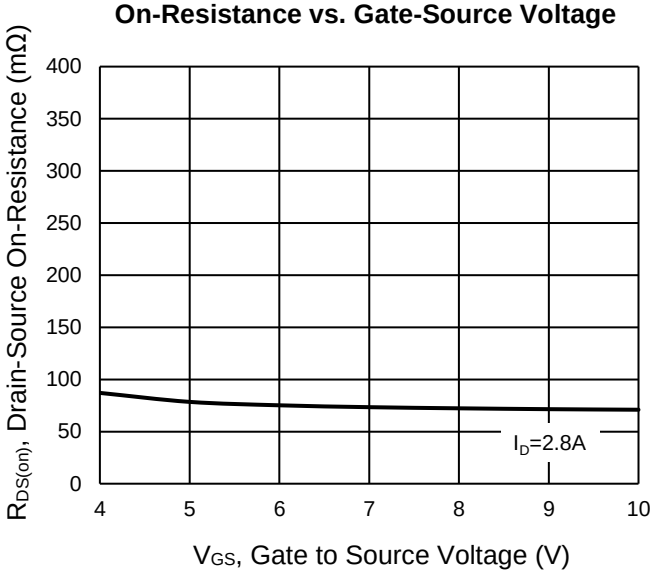
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



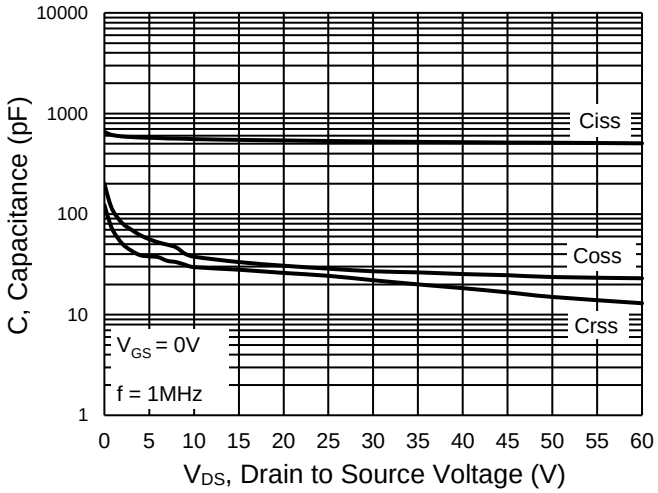
On-Resistance vs. Gate-Source Voltage



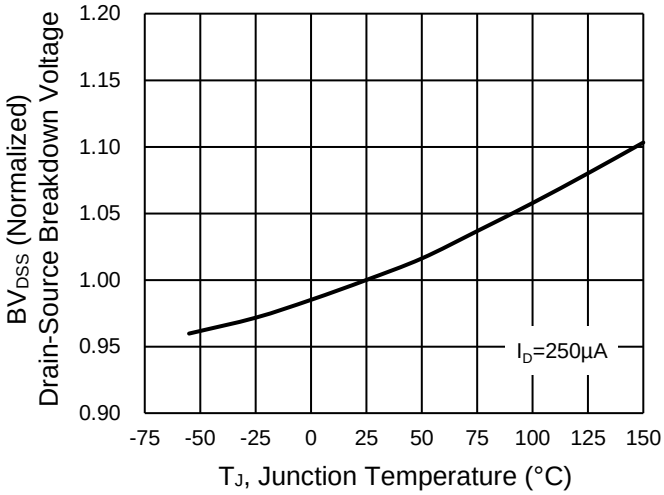
CHARACTERISTICS CURVES (N-Channel)

(T_A = 25°C unless otherwise noted)

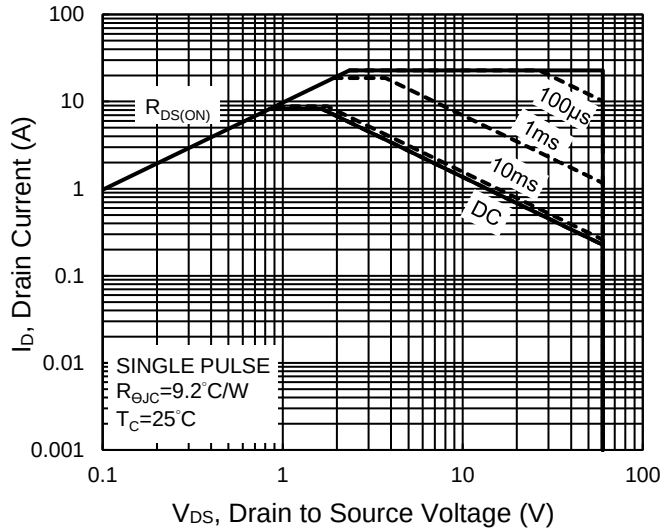
Capacitance vs. Drain-Source Voltage



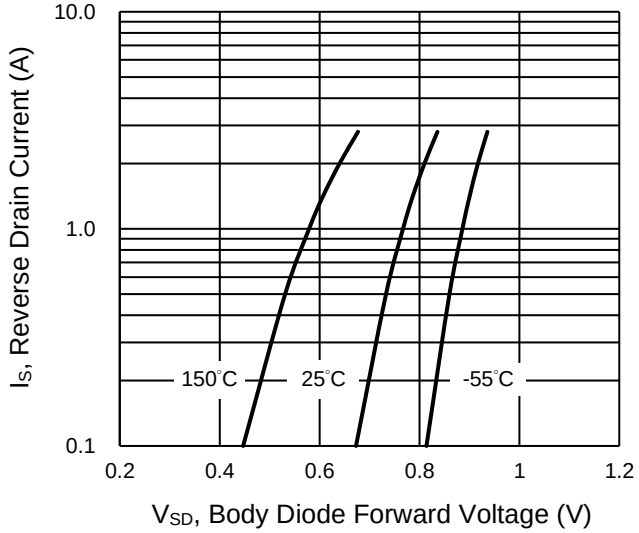
BV_{DSS} vs. Junction Temperature



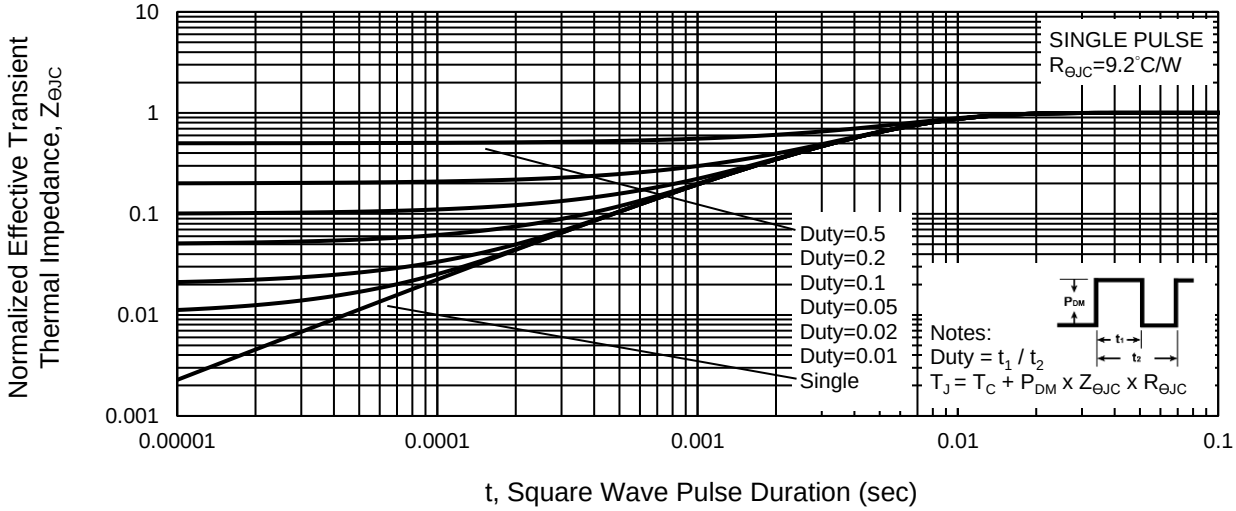
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage



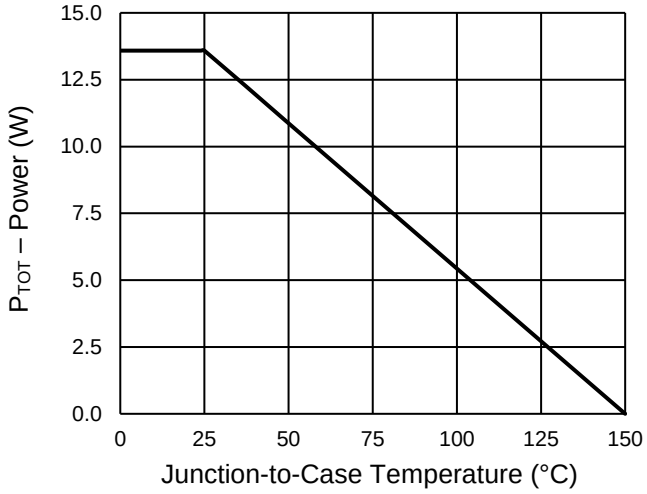
Normalized Thermal Transient Impedance, Junction-to-Case



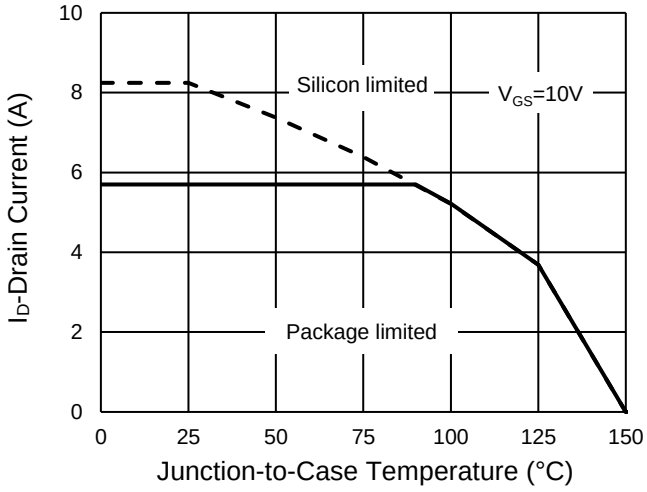
CHARACTERISTICS CURVES (N-Channel)

(T_A = 25°C unless otherwise noted)

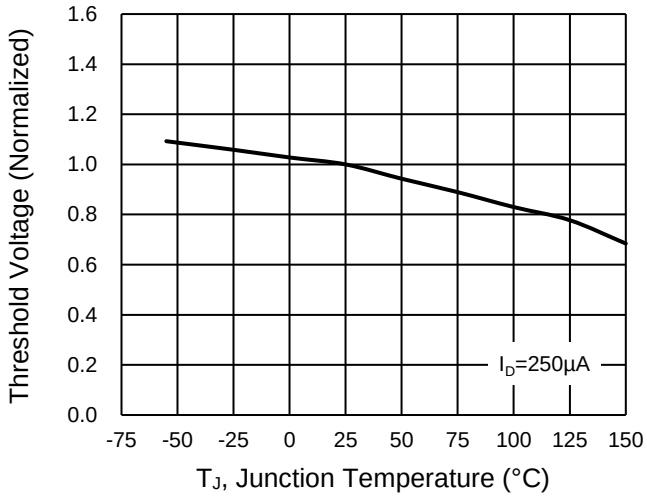
Power Dissipation



Drain Current



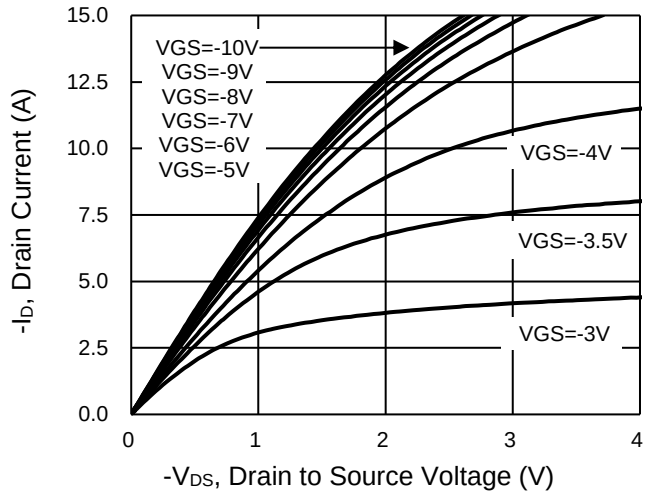
Normalized gate threshold voltage vs Temperature



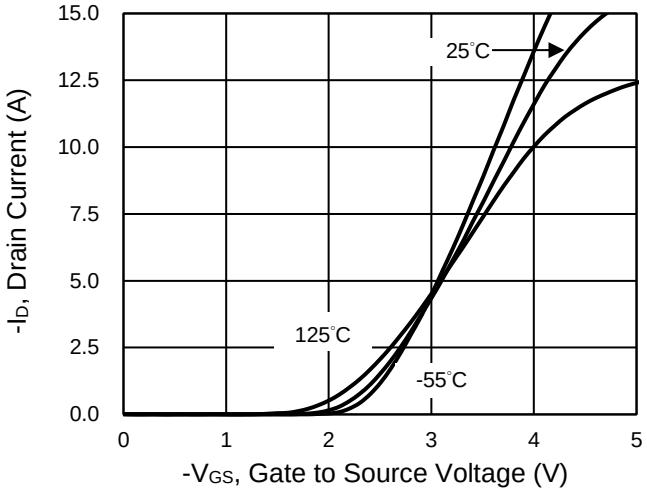
CHARACTERISTICS CURVES (P-Channel)

(T_A = 25°C unless otherwise noted)

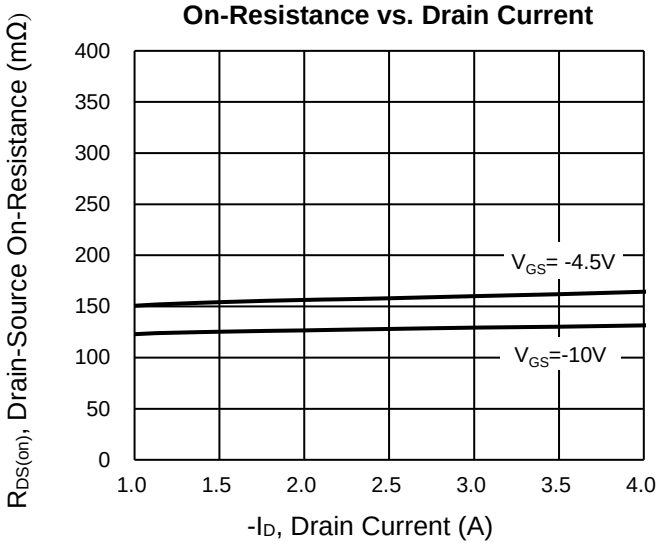
Output Characteristics



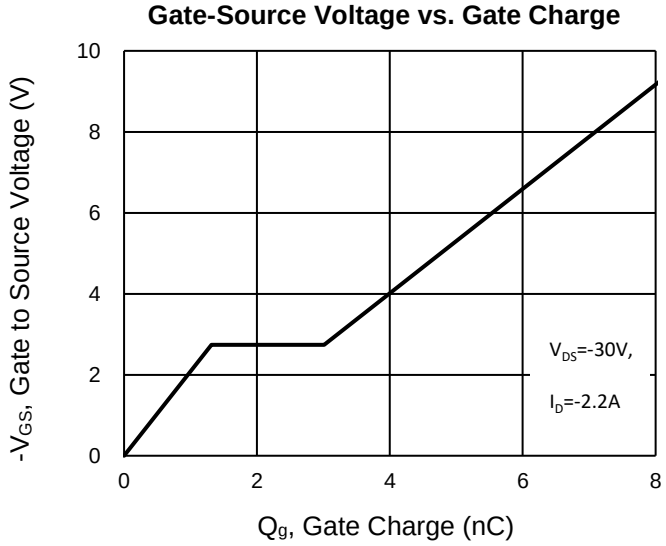
Transfer Characteristics



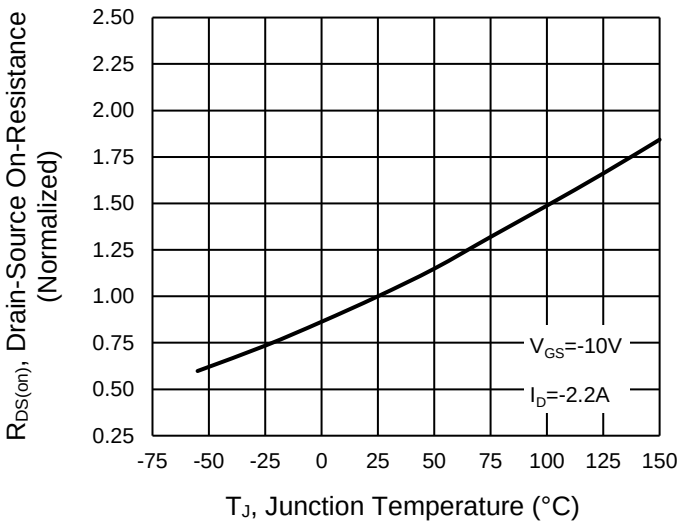
On-Resistance vs. Drain Current



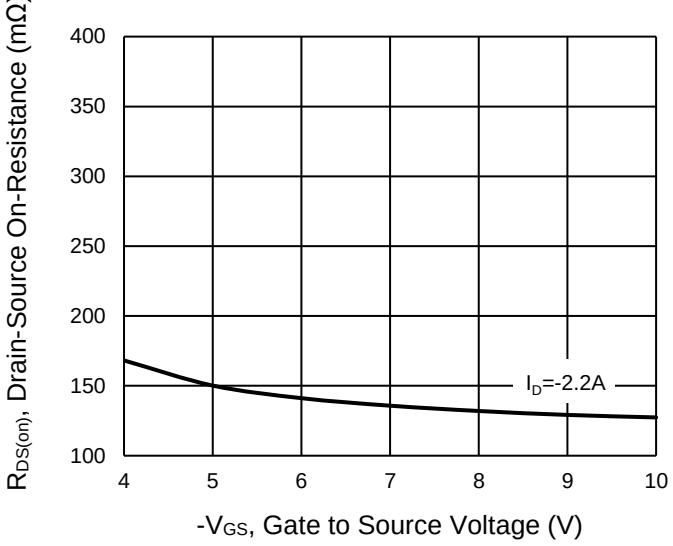
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



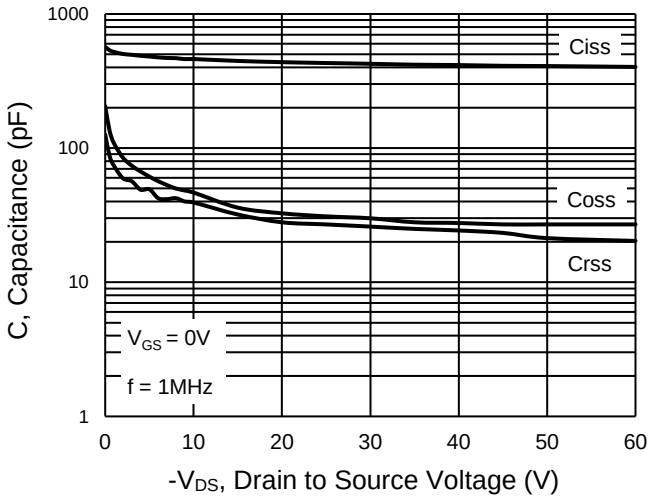
On-Resistance vs. Gate-Source Voltage



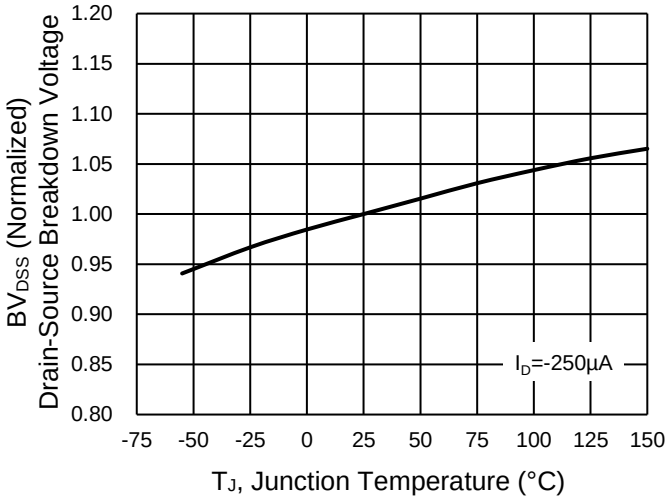
CHARACTERISTICS CURVES (P-Channel)

(T_A = 25°C unless otherwise noted)

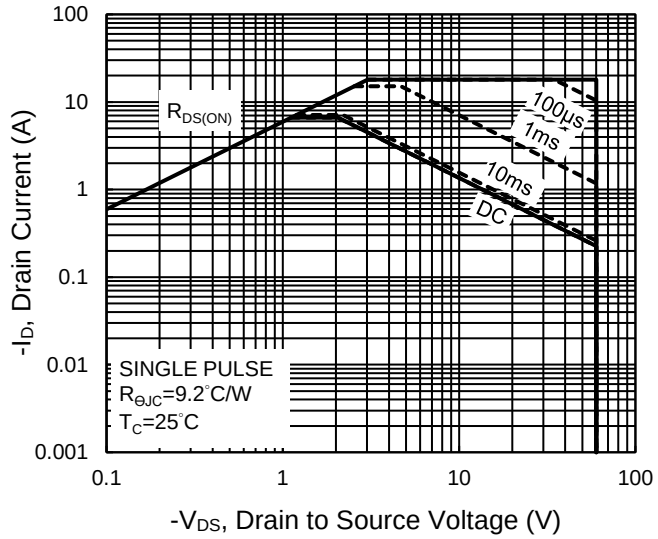
Capacitance vs. Drain-Source Voltage



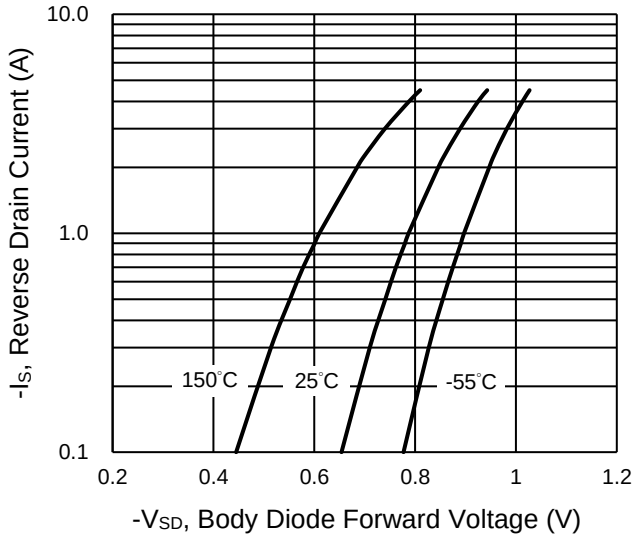
BV_{DSS} vs. Junction Temperature



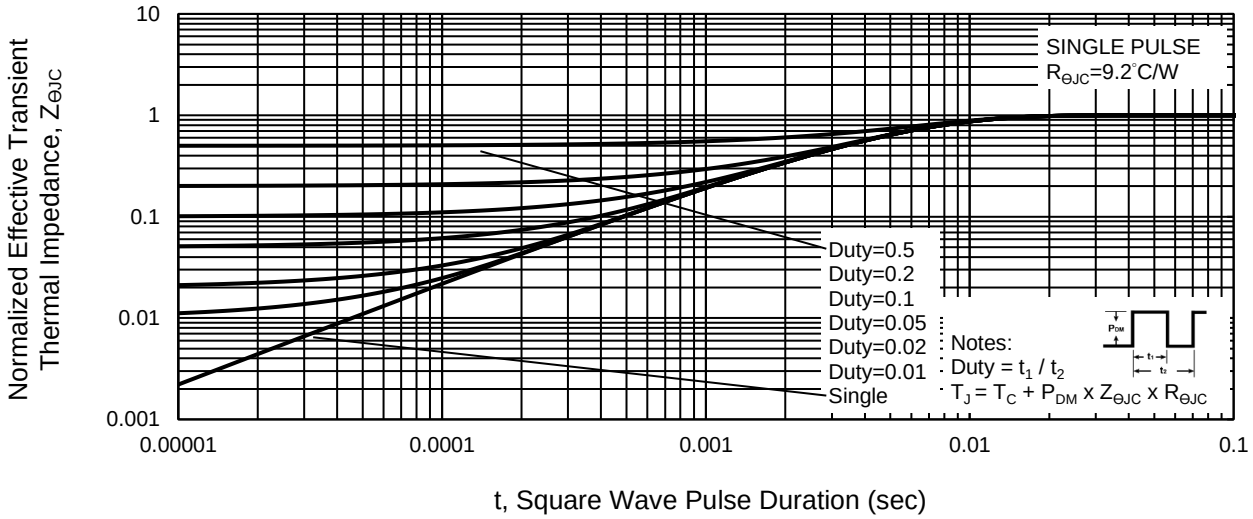
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage



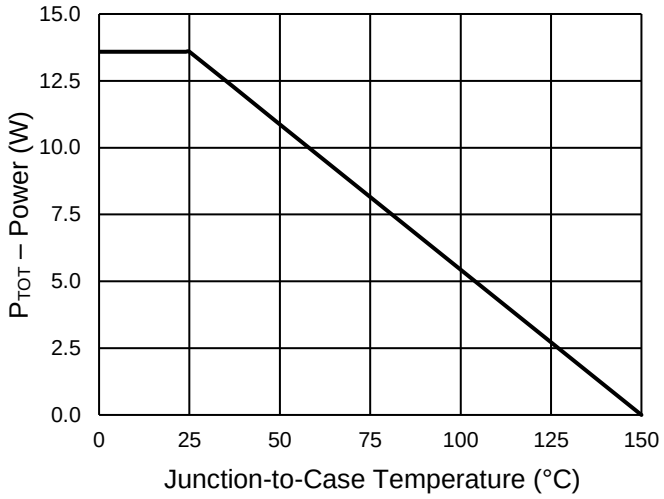
Normalized Thermal Transient Impedance, Junction-to-Case



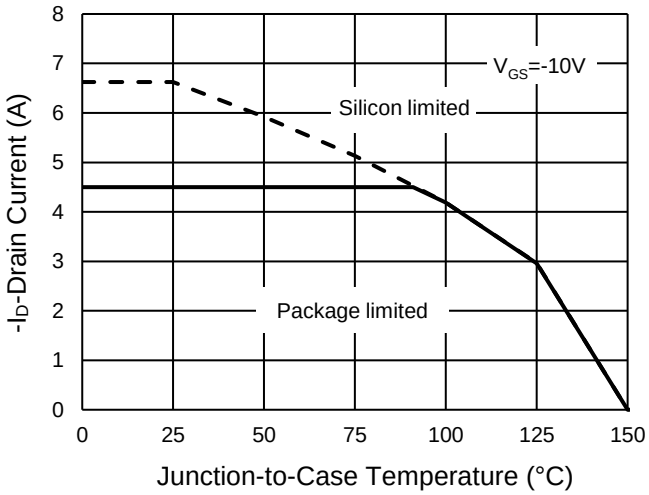
CHARACTERISTICS CURVES (P-Channel)

(T_A = 25°C unless otherwise noted)

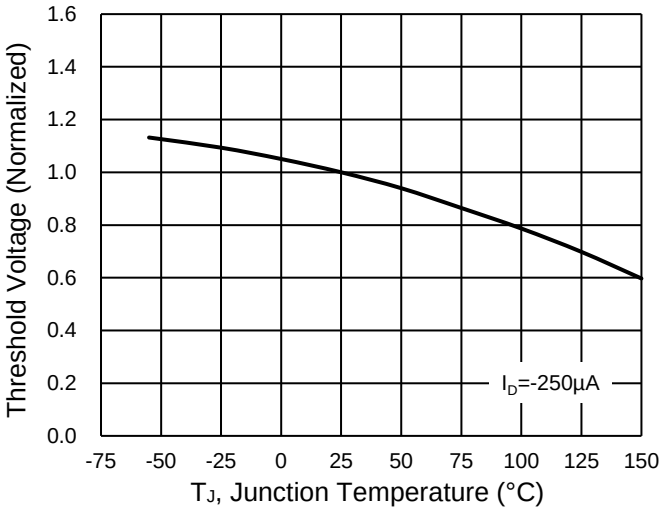
Power Dissipation



Drain Current

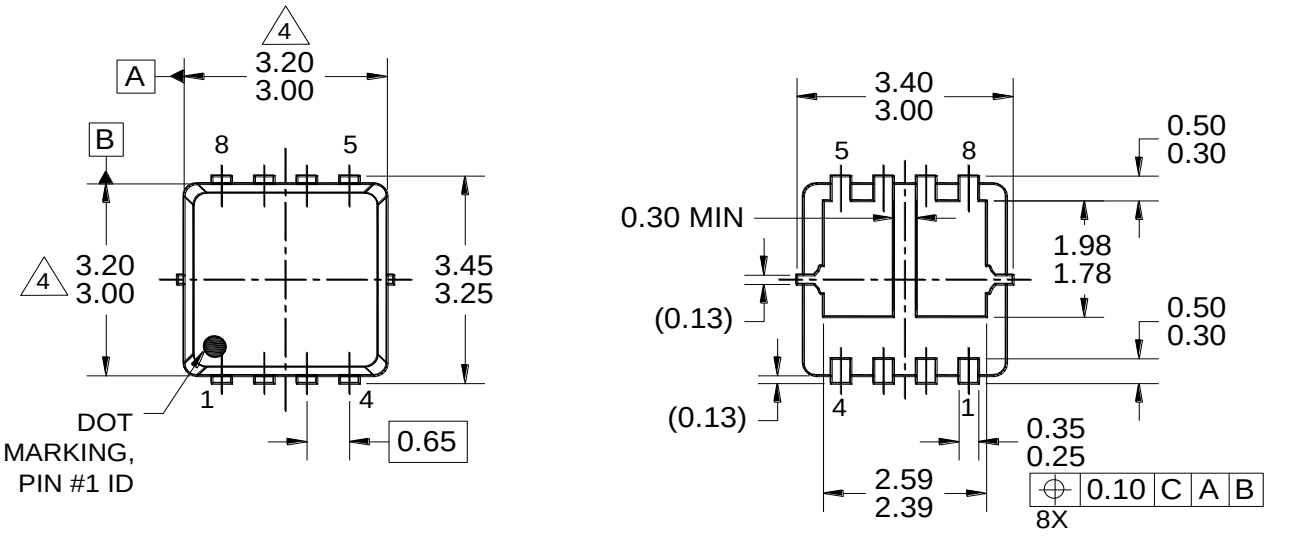


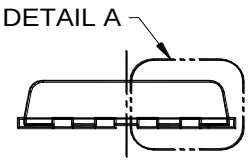
Normalized gate threshold voltage vs Temperature

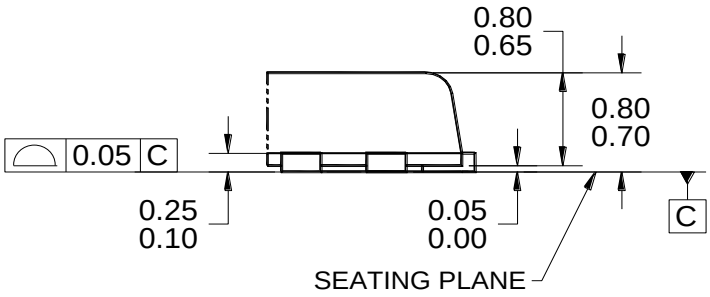


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

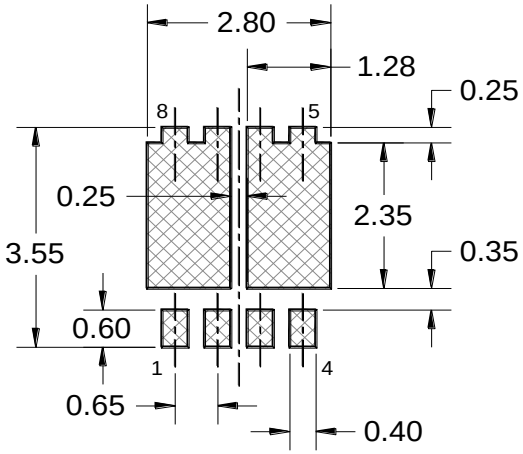
PDFN33 Dual



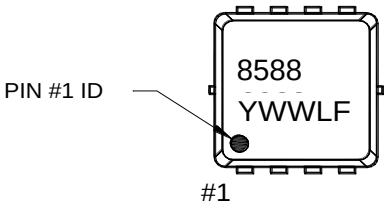




DETAIL A
(SCALE 2:1)



SUGGESTED PAD
LAYOUT



MARKING DIAGRAM

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PACKAGE OUTLINE REFERENCE: EIAJ SC-119.
4. MOLDED PLASTIC BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
5. DWG NO. REF: HQ2SD07-PDFN33D-019 REV A.

Y = YEAR CODE
WW = WEEK CODE (01 ~ 52)
L = LOT CODE (1 ~ 9, A ~ Z)
F = FACTORY CODE

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