

## N and P-Channel 30V (D-S) Power MOSFET

### FEATURES

- Low gate charge for fast power switching
- 100% UIS and  $R_g$  tested
- RoHS Compliant
- Halogen-free

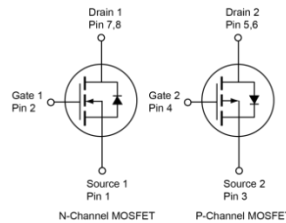
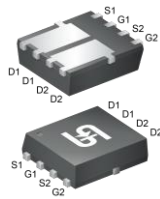
### APPLICATIONS

- DC-DC Converters
- Motor Drives

KEY PERFORMANCE PARAMETERS			
PARAMETER	TYPE	VALUE	UNIT
$V_{DS}$	N-ch	30	V
	P-ch	-30	
$R_{DS(on)}$ (max)	N-ch	$V_{GS} = 10V$	17
		$V_{GS} = 4.5V$	24
	P-ch	$V_{GS} = -10V$	33
		$V_{GS} = -4.5V$	46
$Q_g$	N-ch	16	nC
	P-ch	21	



PDFN33 Dual



Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ C$ unless otherwise noted)					
PARAMETER		SYMBOL	N-ch	P-ch	UNIT
Drain-Source Voltage		$V_{DS}$	30	-30	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	$\pm 25$	V
Continuous Drain Current, Silicon limited	$T_C = 25^\circ C$	$I_D$	29	-24	A
Continuous Drain Current (Note 1)	$T_C = 25^\circ C$	$I_D$	5.7	-4.5	A
	$T_A = 25^\circ C$		5.7	-4.5	
Pulsed Drain Current (Note 2)		$I_{DM}$	22.8	-18	A
Single Pulse Avalanche Current (Note 3)		$I_{AS}$	12	-14	A
Single Pulse Avalanche Energy (Note 3)		$E_{AS}$	22	30	mJ
Total Power Dissipation	$T_C = 25^\circ C$	$P_D$	21	21	W
	$T_C = 125^\circ C$		4.2	4.2	
Operating Junction and Storage Temperature Range		$T_J, T_{STG}$	- 55 to +150		$^\circ C$

THERMAL PERFORMANCE			
PARAMETER	SYMBOL	MAXIMUM	UNIT
Thermal Resistance – Junction to Case	$R_{\theta JC}$	5.9	$^\circ C/W$
Thermal Resistance – Junction to Ambient (Note 4)	$R_{\theta JA}$	81	

### NOTE:

1. Package current limit.
2. Pulse Width  $\leq 100\mu s$ .
3.  $L = 0.3mH$ ,  $V_{GS} = 10V$ ,  $R_G = 25\Omega$ , Starting  $T_J = 25^\circ C$ .
4. Device on a PCB FR4 with 1 in<sup>2</sup> (single layer, 2 oz thick) copper area for drain connection.

<b>ELECTRICAL SPECIFICATIONS</b> ( $T_A = 25^\circ\text{C}$ unless otherwise noted)							
PARAMETER	CONDITIONS	SYMBOL	TYPE	MIN	TYP	MAX	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu\text{A}$	$BV_{DSS}$	N-ch	30	--	--	V
	$V_{GS} = 0V, I_D = -250\mu\text{A}$		P-ch	-30	--	--	
Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	$V_{GS(TH)}$	N-ch	1	1.5	2.5	V
	$V_{GS} = V_{DS}, I_D = -250\mu\text{A}$		P-ch	-1	-1.5	-2.5	
Gate-Source Leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$	$I_{GSS}$	N-ch	--	--	$\pm 100$	nA
	$V_{GS} = \pm 25V, V_{DS} = 0V$		P-ch	--	--	$\pm 100$	nA
Drain-Source Leakage Current	$V_{GS} = 0V, V_{DS} = 30V$	$I_{DSS}$	N-ch	--	--	1	$\mu\text{A}$
	$V_{GS} = 0V, V_{DS} = 30V$ $T_J = 125^\circ\text{C}$			--	--	100	
	$V_{GS} = 0V, V_{DS} = -30V$		P-ch	--	--	-1	
	$V_{GS} = 0V, V_{DS} = -30V$ $T_J = 125^\circ\text{C}$			--	--	-100	
Drain-Source On-State Resistance (Note 5)	$V_{GS} = 10V, I_D = 2.8A$	$R_{DS(on)}$	N-ch	--	13	17	m $\Omega$
	$V_{GS} = 4.5V, I_D = 2.8A$			--	16	24	
	$V_{GS} = -10V, I_D = -2.2A$		P-ch	--	25	33	
	$V_{GS} = -4.5V, I_D = -2.2A$			--	35	46	
Forward Transconductance (Note 5)	$V_{DS} = 10V, I_D = 0.7A$	$g_{fs}$	N-ch	--	5.8	--	S
	$V_{DS} = -10V, I_D = -0.6A$		P-ch	--	4.4	--	
<b>Dynamic (Note 6)</b>							
Total Gate Charge	N-ch $V_{DS} = 15V, I_D = 5.7A$	$Q_g$	N-ch	--	16	--	nC
			P-ch	--	21	--	
Gate-Source Charge	$V_{GS} = 10V$	$Q_{gs}$	N-ch	--	1.9	--	
			P-ch	--	3	--	
Gate-Drain Charge	$V_{DS} = -20V, I_D = -4.5A$ $V_{GS} = -10V$	$Q_{gd}$	N-ch	--	3.1	--	
			P-ch	--	4.8	--	
Input Capacitance	N-ch $V_{GS} = 0V, V_{DS} = 15V$	$C_{iss}$	N-ch	--	741	--	pF
			P-ch	--	1088	--	
Output Capacitance	$f = 1.0\text{MHz}$	$C_{oss}$	N-ch	--	175	--	
			P-ch	--	182	--	
Reverse Transfer Capacitance	$V_{GS} = 0V, V_{DS} = -15V$ $f = 1.0\text{MHz}$	$C_{rss}$	N-ch	--	81	--	
			P-ch	--	142	--	
Gate Resistance	$f = 1.0\text{MHz}$	$R_g$	N-ch	--	2.4	--	$\Omega$
			P-ch	--	13	--	

**Notes:**

5. Pulse test: Pulse Width  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$ .
6. Defined by design. Not subject to production test.

<b>ELECTRICAL SPECIFICATIONS</b> ( $T_A = 25^\circ\text{C}$ unless otherwise noted)							
PARAMETER	CONDITIONS	SYMBOL	TYPE	MIN	TYP	MAX	UNIT
<b>Switching</b> (Note 7)							
Turn-On Delay Time	N-ch $V_{GS} = 10\text{V}$ , $V_{DS} = 15\text{V}$ , $I_D = 5.7\text{A}$ , $R_G = 3.3\Omega$  P-ch $V_{GS} = -10\text{V}$ , $V_{DS} = -20\text{V}$ , $I_D = -4.5\text{A}$ , $R_G = 3.3\Omega$	$t_{d(on)}$	N-ch	--	5.8	--	ns
			P-ch	--	6.2	--	
Turn-On Rise Time		$t_r$	N-ch	--	38	--	
			P-ch	--	25	--	
Turn-Off Delay Time		$t_{d(off)}$	N-ch	--	22	--	
			P-ch	--	50	--	
Turn-Off Fall Time	$t_f$	N-ch	--	5.2	--		
		P-ch	--	46	--		
<b>Source-Drain Diode</b>							
Forward Voltage (Note 5)	$V_{GS} = 0\text{V}$ , $I_S = 2.8\text{A}$	$V_{SD}$	N-ch	--	--	1	V
	$V_{GS} = 0\text{V}$ , $I_S = -2.2\text{A}$		P-ch	--	--	-1	
Reverse Recovery Time	N-ch $I_S = 5.7\text{A}$ , $dI/dt = 100\text{A}/\mu\text{s}$	$t_{rr}$	N-ch	--	12	--	ns
			P-ch	--	22	--	
Reverse Recovery Charge	P-ch $I_S = -4.5\text{A}$ , $dI/dt = 100\text{A}/\mu\text{s}$	$Q_{rr}$	N-ch	--	4.2	--	nC
			P-ch	--	7.8	--	

**Notes:**

7. Switching time is essentially independent of operating temperature.

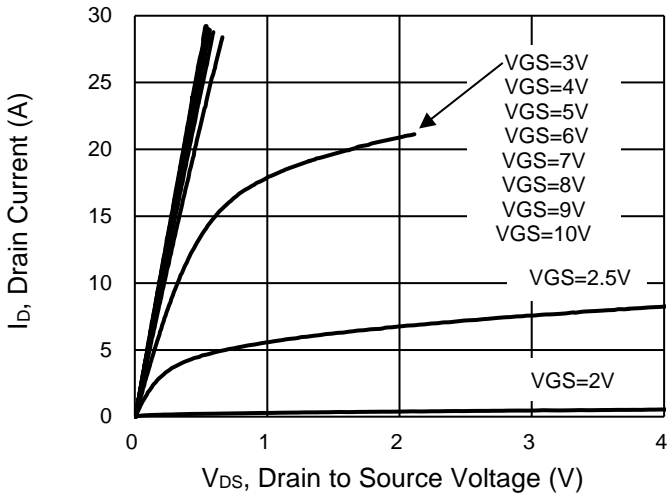
## ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TSM8568CV RGG	PDFN33 Dual	5,000pcs / 13" Reel

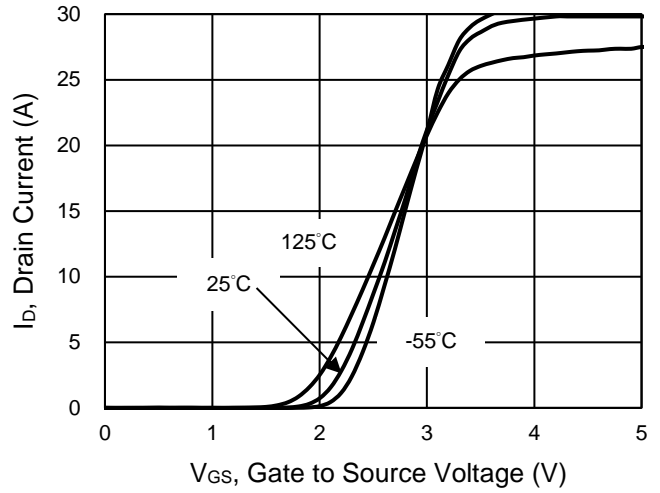
**CHARACTERISTICS CURVES (N-Channel)**

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

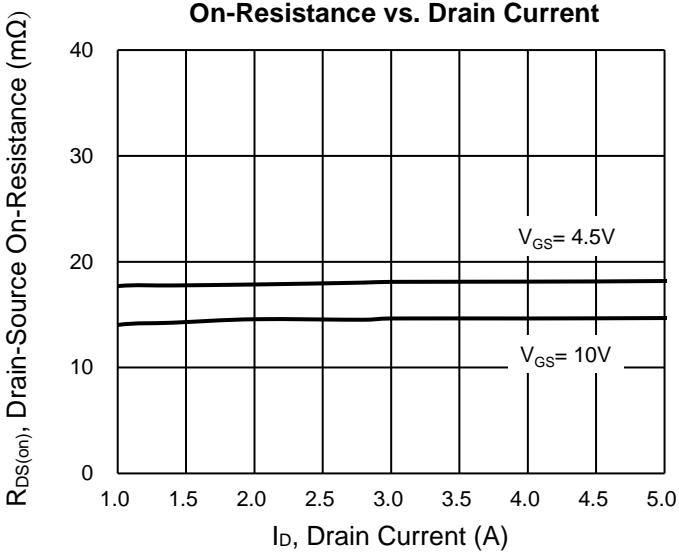
**Output Characteristics**



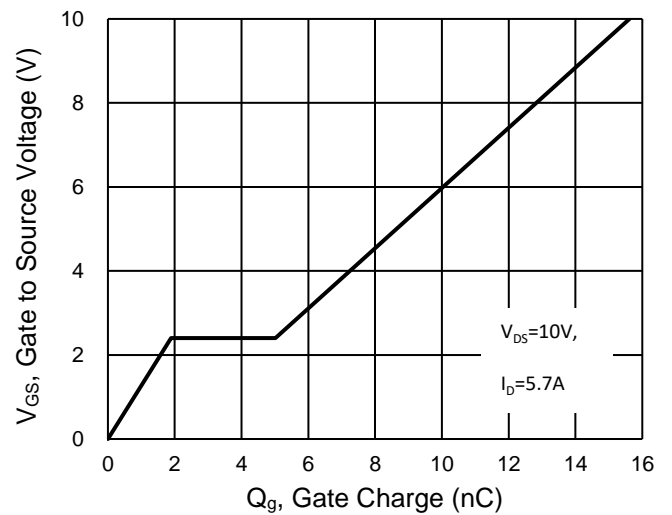
**Transfer Characteristics**



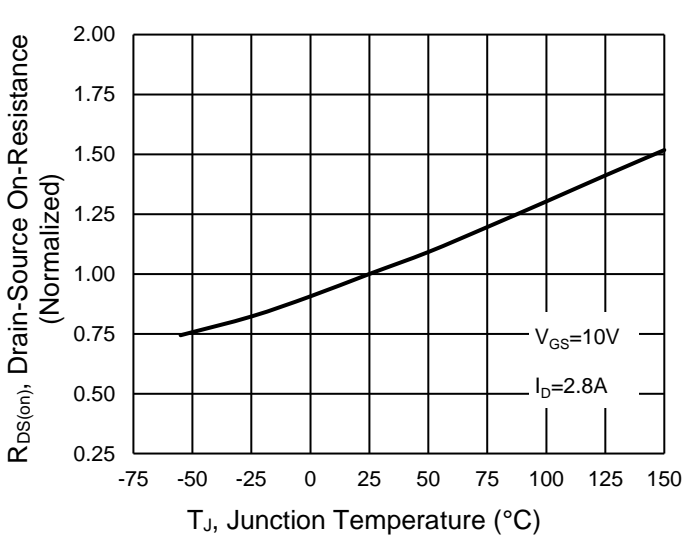
**On-Resistance vs. Drain Current**



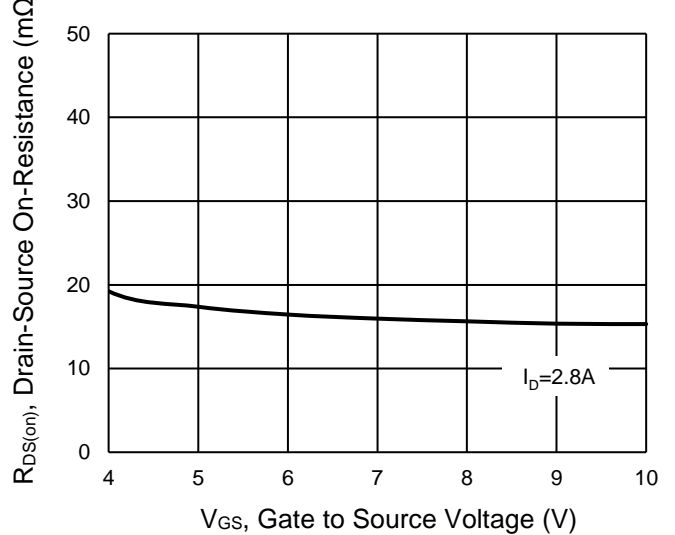
**Gate-Source Voltage vs. Gate Charge**



**On-Resistance vs. Junction Temperature**

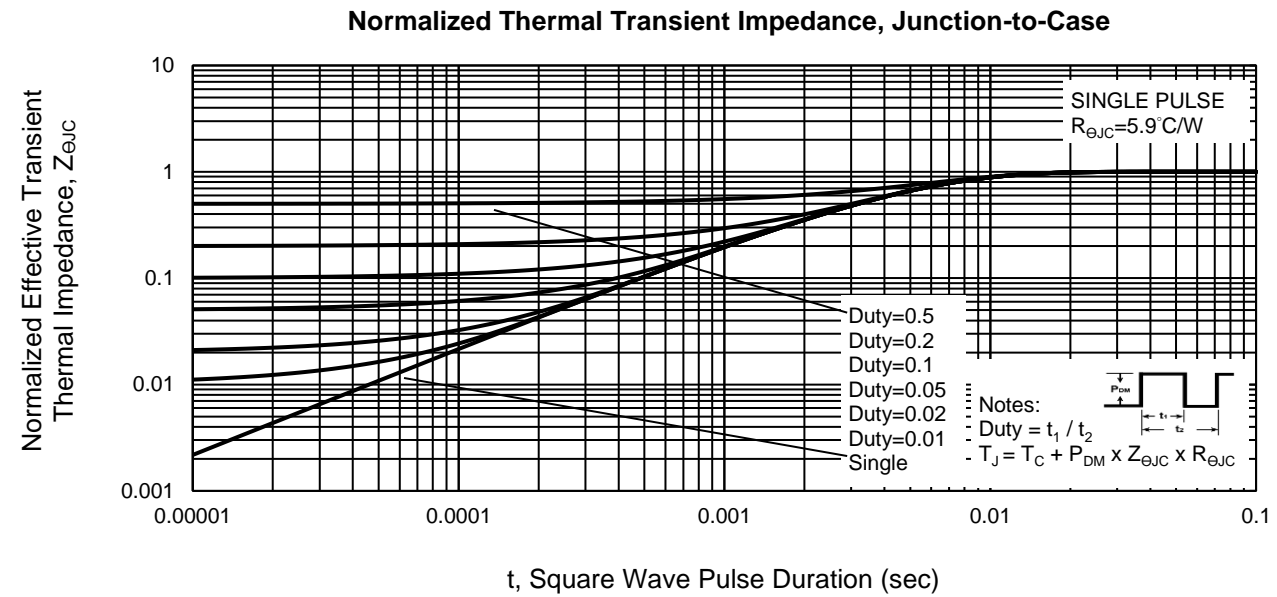
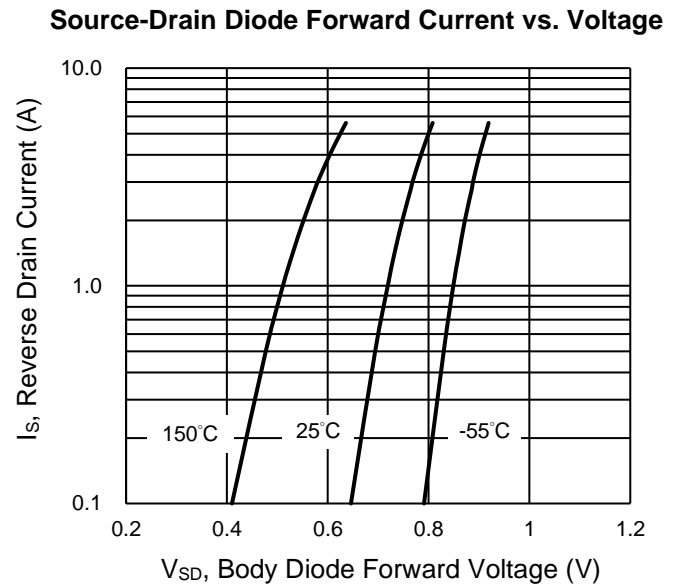
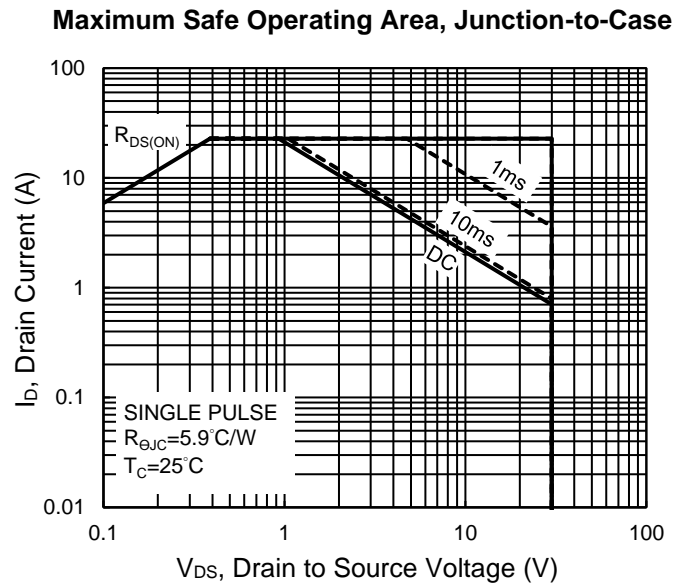
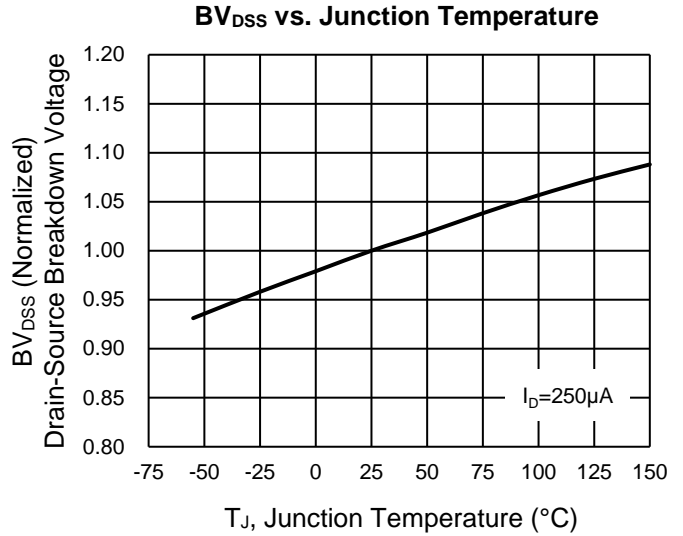
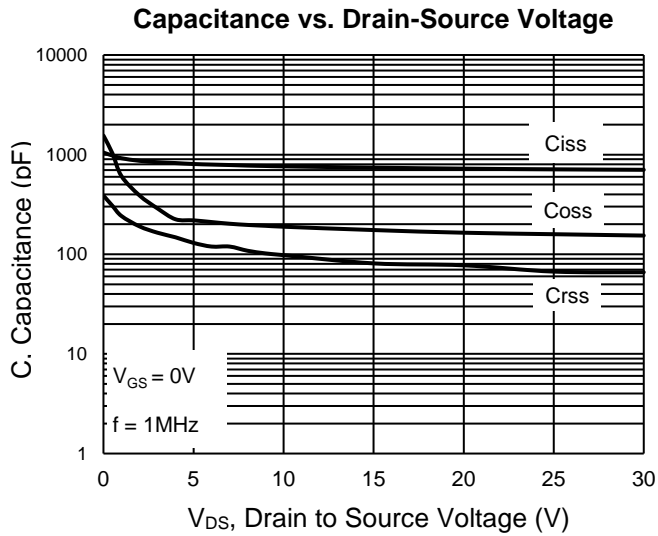


**On-Resistance vs. Gate-Source Voltage**



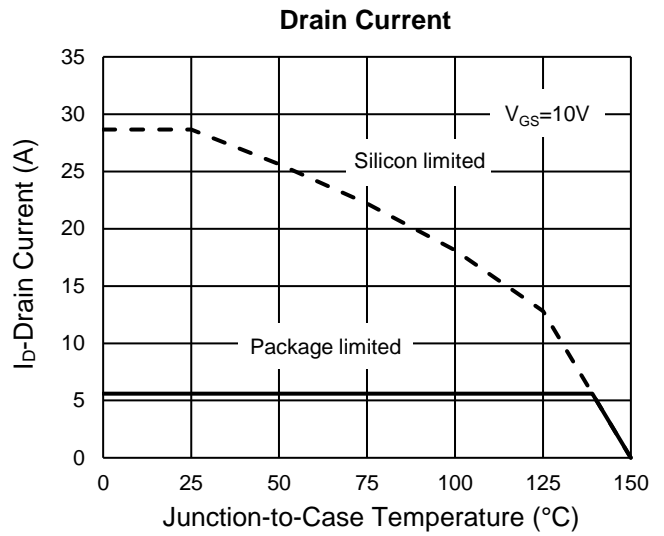
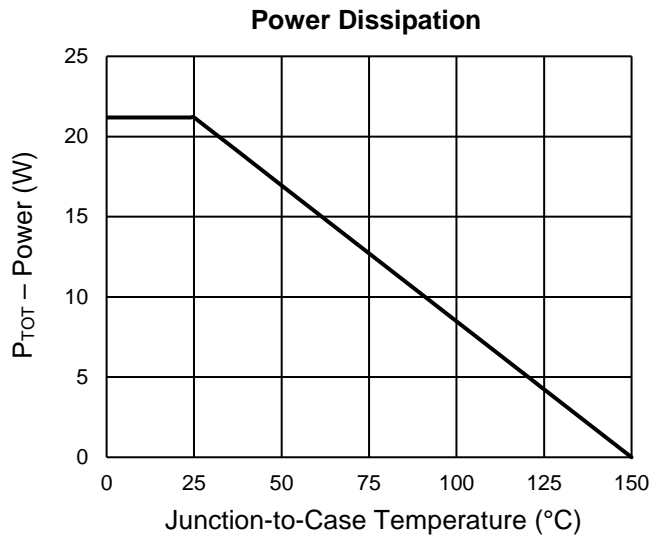
**CHARACTERISTICS CURVES (N-Channel)**

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

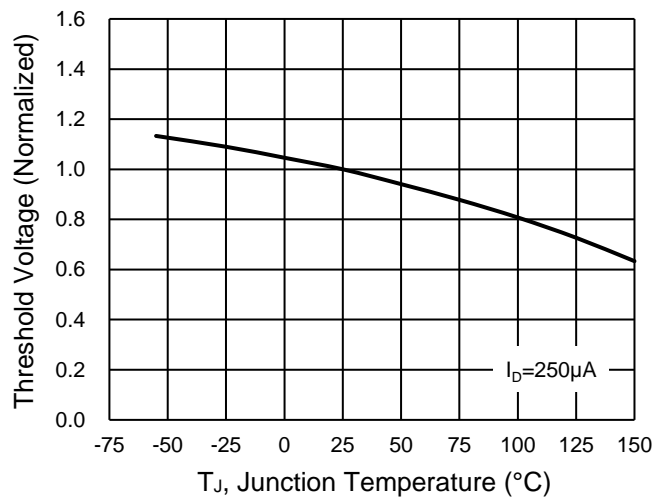


**CHARACTERISTICS CURVES (N-Channel)**

( $T_A = 25^\circ\text{C}$  unless otherwise noted)



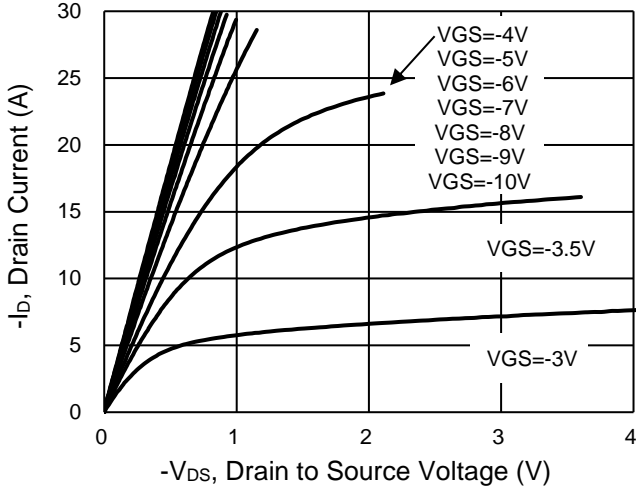
**Normalized gate threshold voltage vs Temperature**



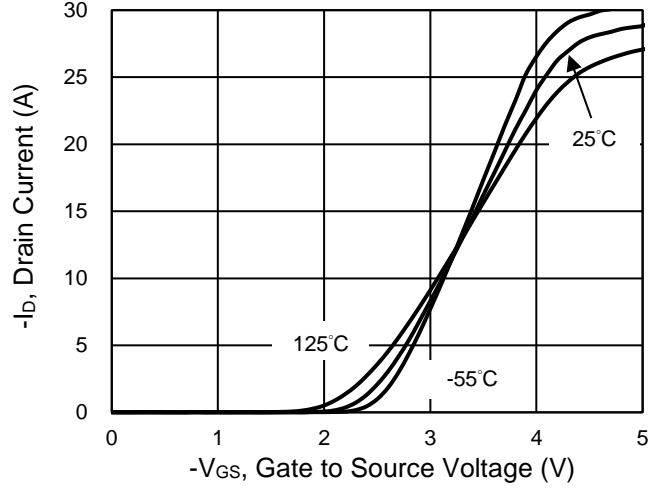
**CHARACTERISTICS CURVES (P-Channel)**

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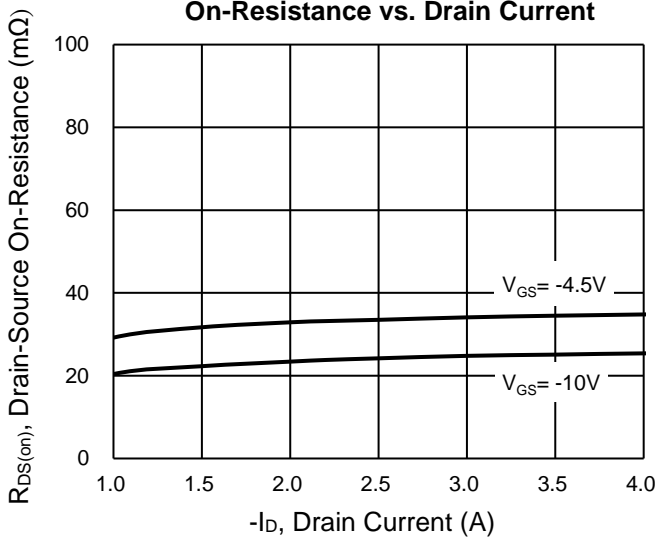
**Output Characteristics**



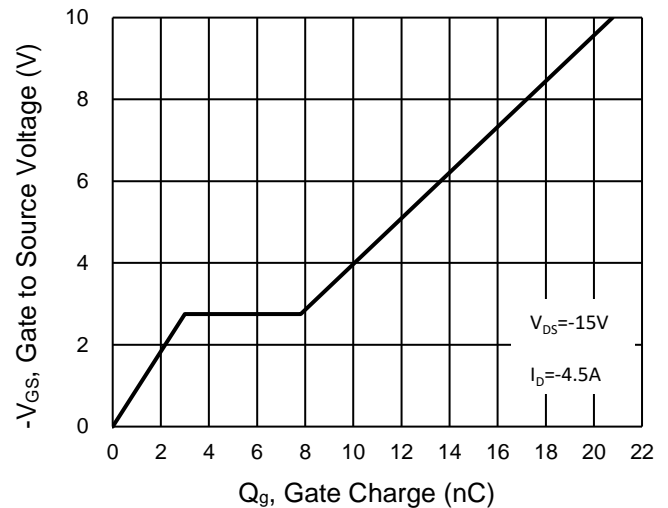
**Transfer Characteristics**



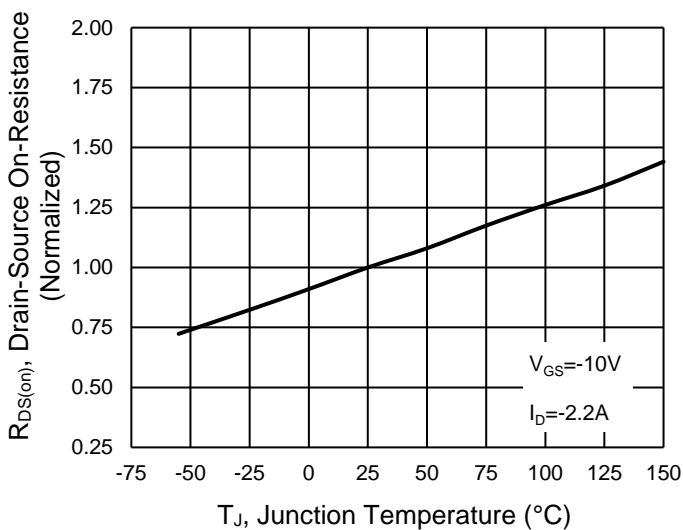
**On-Resistance vs. Drain Current**



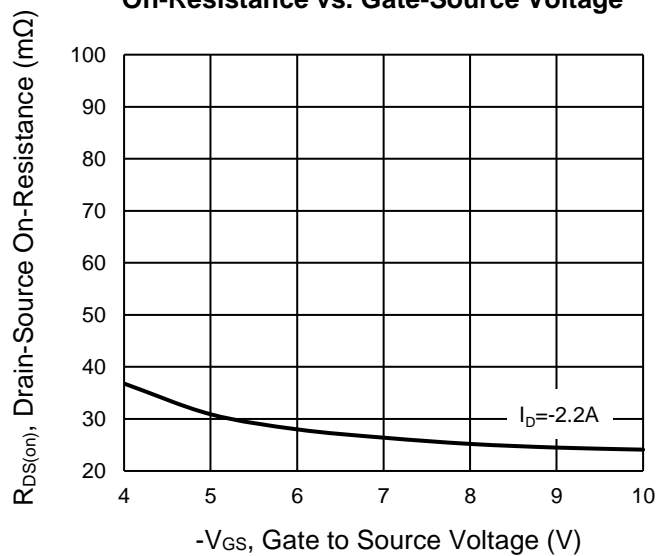
**Gate-Source Voltage vs. Gate Charge**



**On-Resistance vs. Junction Temperature**

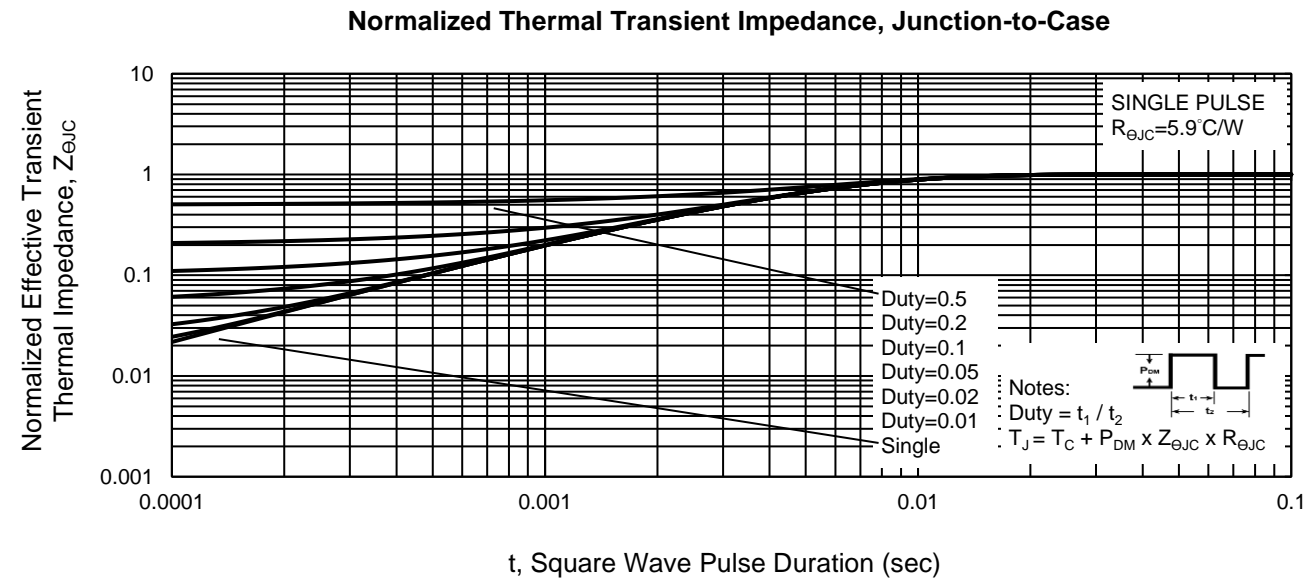
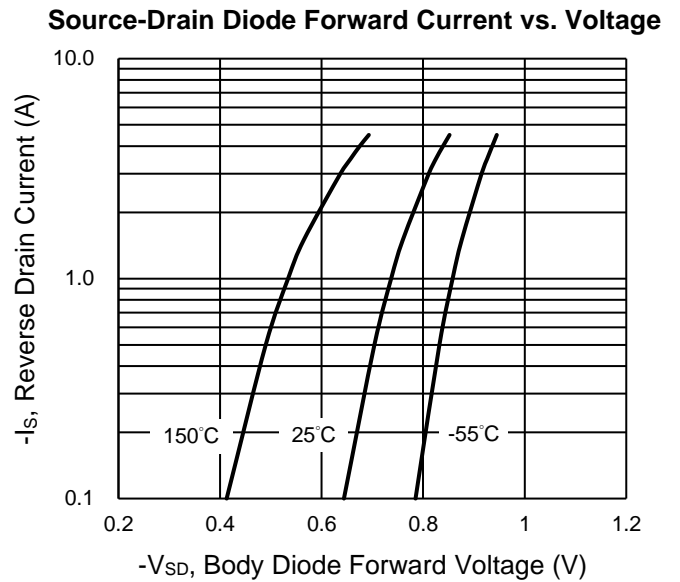
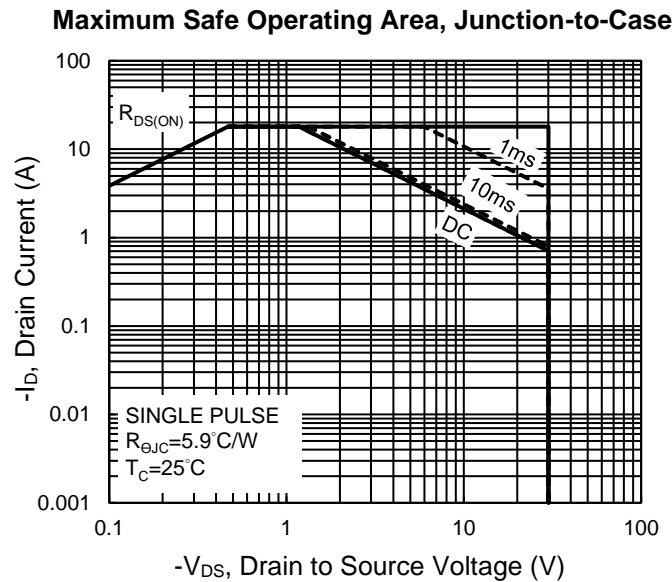
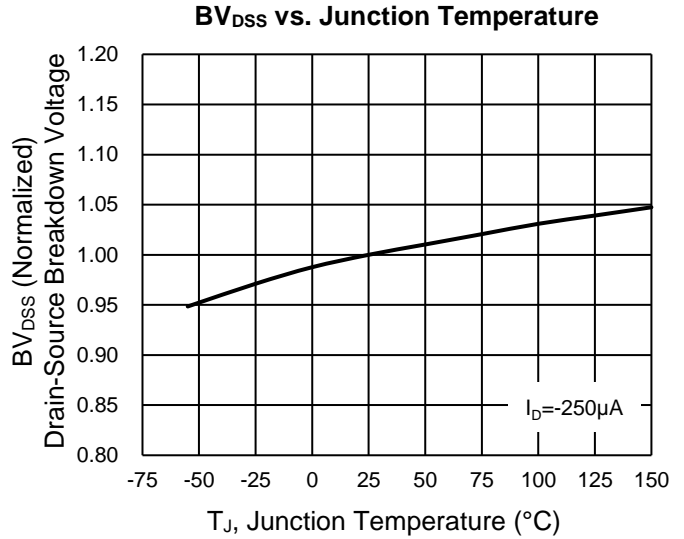
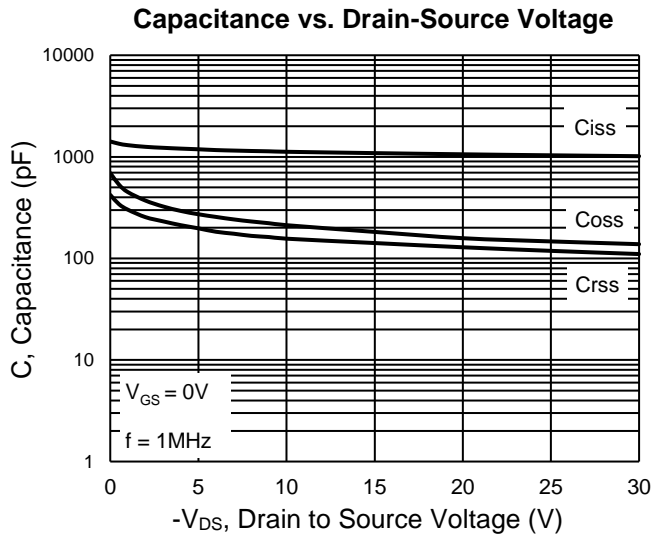


**On-Resistance vs. Gate-Source Voltage**



**CHARACTERISTICS CURVES (P-Channel)**

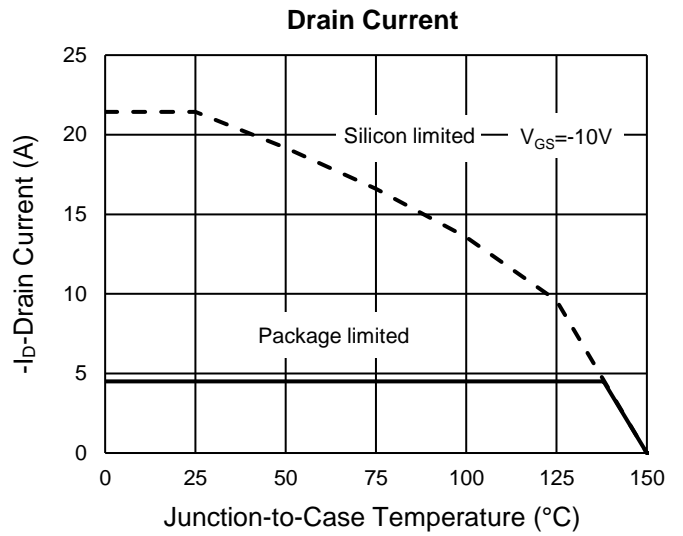
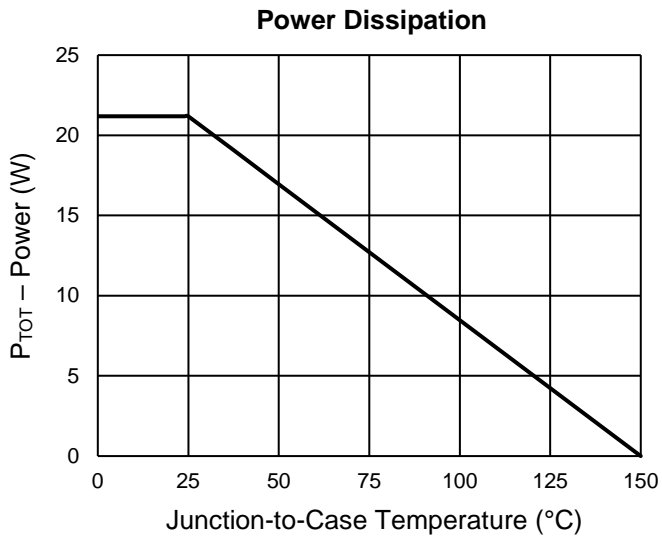
( $T_A = 25^\circ\text{C}$  unless otherwise noted)



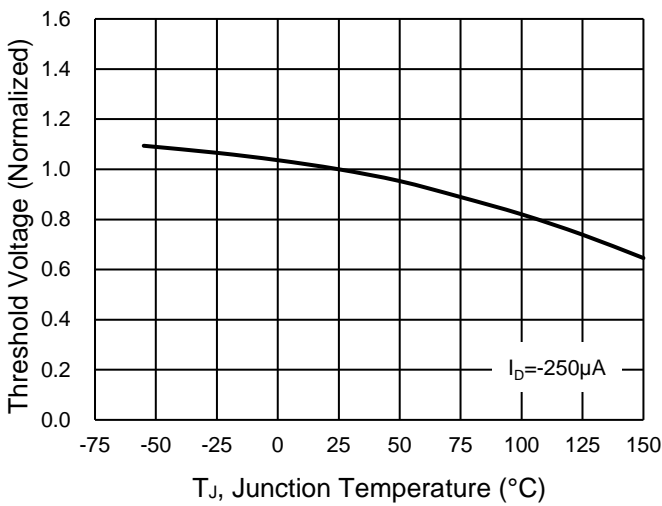


**CHARACTERISTICS CURVES (P-Channel)**

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

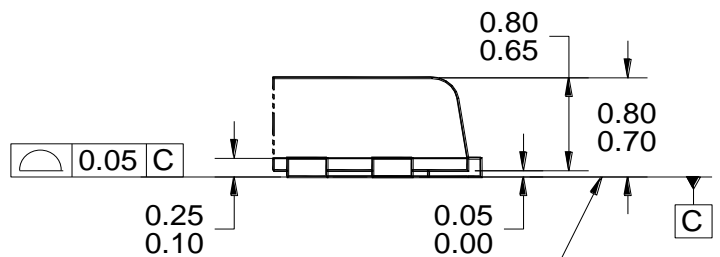
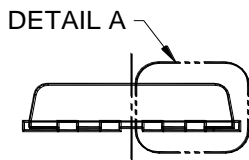
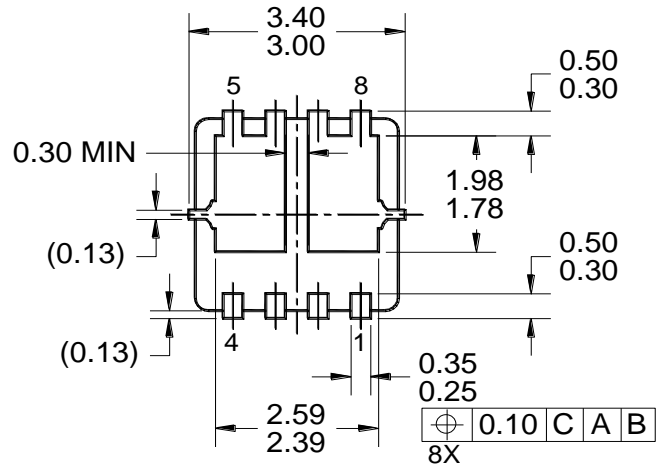
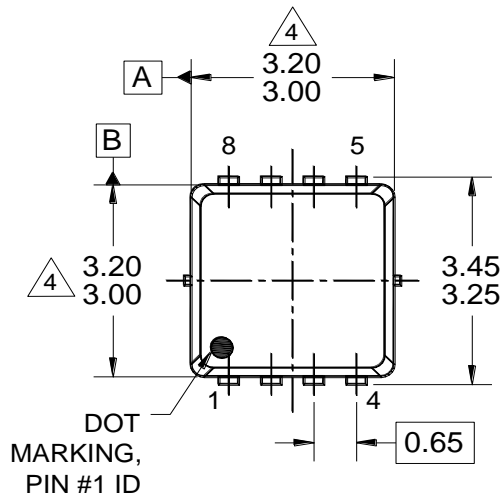


**Normalized gate threshold voltage vs Temperature**

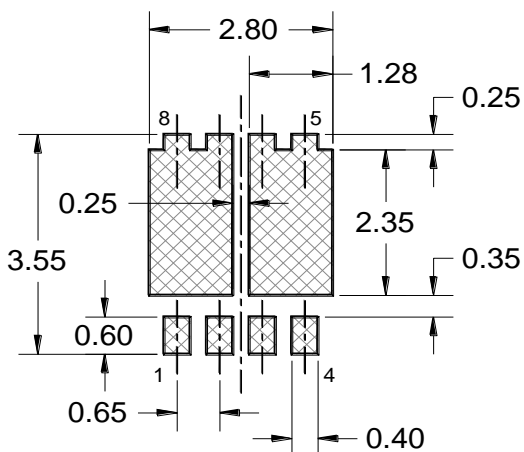


**PACKAGE OUTLINE DIMENSIONS** (Unit: Millimeters)

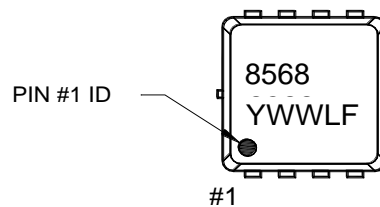
**PDFN33 Dual**



DETAIL A  
(SCALE 2:1)



SUGGESTED PAD  
LAYOUT



MARKING DIAGRAM

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PACKAGE OUTLINE REFERENCE: EIAJ SC-119.
4. MOLDED PLASTIC BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
5. DWG NO. REF: HQ2SD07-PDFN33D-019 REV A.

- Y = YEAR CODE  
 WW = WEEK CODE (01 ~ 52)  
 L = LOT CODE (1 ~ 9, A ~ Z)  
 F = FACTORY CODE

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