

## N-Channel Power MOSFET

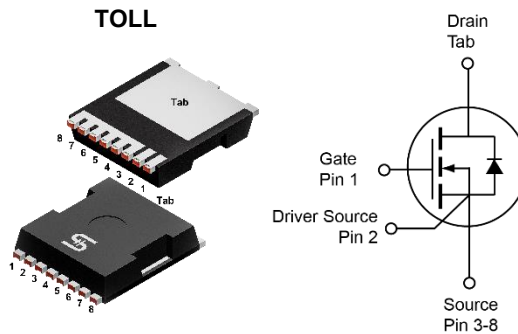
### FEATURES

- Latest super-junction technology
- Low gate charge capacitance
- High gate noise immunity
- TOLL package offers good thermal performance
- The driver source pin (Kelvin-source) helps reduce switching losses
- RoHS compliant
- Halogen-free

### APPLICATIONS

- Switching power supply
- HV motor driver

KEY PERFORMANCE PARAMETERS		
PARAMETER	VALUE	UNIT
$V_{DS} @ T_{j,max}$	650	V
$R_{DS(on)} (max)$	84	mΩ
$Q_{g,typ}$	69	nC



Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	600	V
Gate-Source Voltage	$V_{GS}$	static	$\pm 20$
		AC( $f > 1\text{Hz}$ )	$\pm 30$
Continuous Drain Current	$I_D$	47	A
Pulsed Drain Current (Note 1)	$I_{DM}$	141	A
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	$P_D$	431	W
Single Pulse Avalanche Energy (Note 2)	$E_{AS}$	208	mJ
Single Pulse Avalanche Current (Note 2)	$I_{AS}$	2.8	A
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	- 55 to +150	$^\circ\text{C}$

THERMAL PERFORMANCE			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	0.29	$^\circ\text{C/W}$
Junction to Ambient Thermal Resistance (Note 3)	$R_{\theta JA}$	45	$^\circ\text{C/W}$

#### Notes:

1. Pulse Width  $\leq 100\mu\text{s}$ .
2.  $L \doteq 50\text{mH}$ ,  $R_G = 25\Omega$ , Starting  $T_J = 25^\circ\text{C}$ .
3. Device on a PCB FR4 with 1 in<sup>2</sup> (single layer, 2 oz thickness) copper area for drain connection.

**ELECTRICAL SPECIFICATIONS** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
<b>Static</b> (Note 4)						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 1mA$	$BV_{DSS}$	600	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 2.9mA$	$V_{GS(TH)}$	4	4.7	6	V
Gate Body Leakage	$V_{GS} = \pm 30V, V_{DS} = 0V$	$I_{GSS}$	--	--	$\pm 100$	nA
Zero Gate Voltage Drain Current	$V_{DS} = 600V, V_{GS} = 0V$	$I_{DSS}$	--	--	100	$\mu A$
Drain-Source On-State Resistance	$V_{GS} = 12V, I_D = 16A$	$R_{DS(on)}$	--	66	82	m $\Omega$
	$V_{GS} = 10V, I_D = 16A$		--	69	84	
<b>Dynamic</b> (Note 5)						
Total Gate Charge	$V_{DS} = 480V, I_D = 47A,$ $V_{GS} = 10V$	$Q_g$	--	69	--	nC
Gate-Source Charge		$Q_{gs}$	--	24	--	
Gate-Drain Charge		$Q_{gd}$	--	40	--	
Input Capacitance	$V_{DS} = 300V, V_{GS} = 0V,$ $f = 100kHz$	$C_{iss}$	--	2908	--	pF
Output Capacitance		$C_{oss}$	--	86	--	
Effective output capacitance energy related	$V_{GS} = 0V$	$C_{o(er)}$	--	151	--	
Effective output capacitance time related	$V_{DS} = 0V$ to 480V	$C_{o(tr)}$	--	738	--	
Gate Resistance	$f = 1.0MHz$	$R_g$	--	1.1	--	$\Omega$
<b>Switching</b> (Note 6)						
Turn-On Delay Time	$V_{DD} = 300V, R_G = 3.3\Omega,$ $I_D = 47A, V_{GS} = 10V$	$t_{d(on)}$	--	43	--	ns
Turn-On Rise Time		$t_r$	--	69	--	
Turn-Off Delay Time		$t_{d(off)}$	--	67	--	
Turn-Off Fall Time		$t_f$	--	44	--	
<b>Source-Drain Diode</b>						
Forward Voltage (Note 4)	$I_S = 16A, V_{GS} = 0V$	$V_{SD}$	--	--	1.5	V
Reverse Recovery Time	$I_S = 23.5A$	$t_{rr}$	--	418	--	ns
Reverse Recovery Charge	$di_F/dt = 100A/\mu s$	$Q_{rr}$	--	9.1	--	$\mu C$

**Notes:**

4. Pulse test: Pulse Width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$ .
5. Defined by design. Not subject to production test.
6. Switching time is essentially independent of operating temperature.

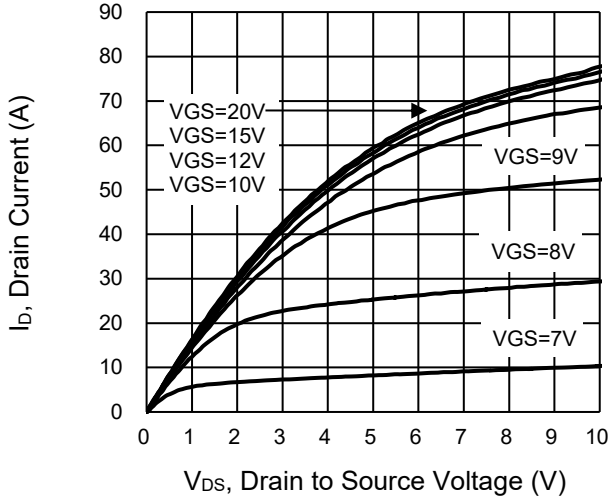
**ORDERING INFORMATION**

ORDERING CODE	PACKAGE	PACKING
TSM60NE084TL RAG	TOLL	2,000pcs / 13" Reel

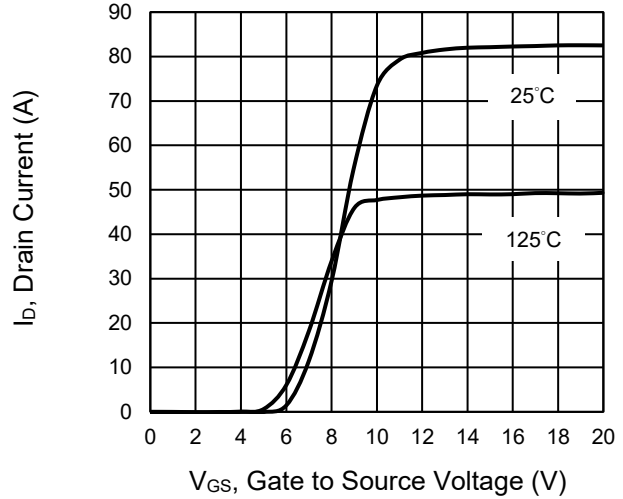
**CHARACTERISTICS CURVES**

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

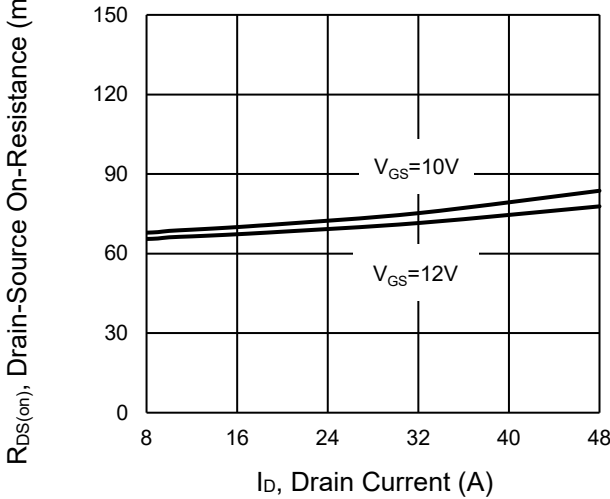
**Output Characteristics**



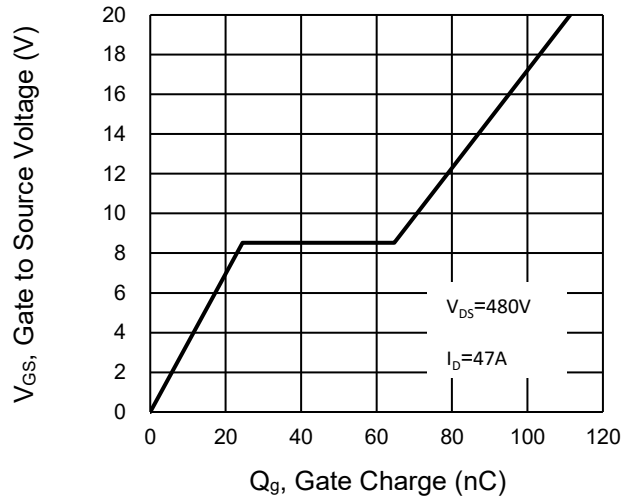
**Transfer Characteristics**



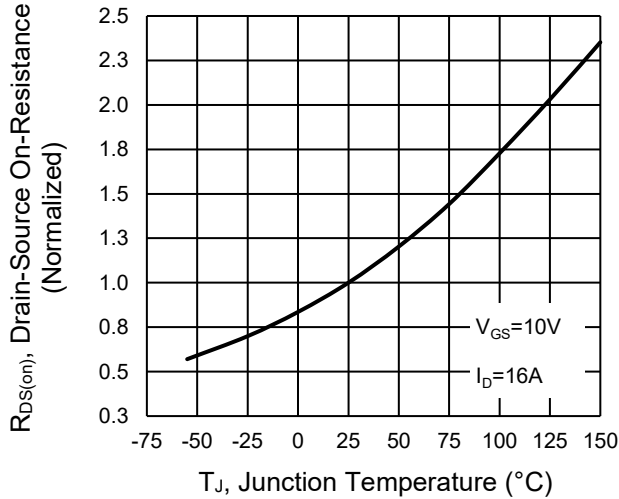
**On-Resistance vs. Drain Current**



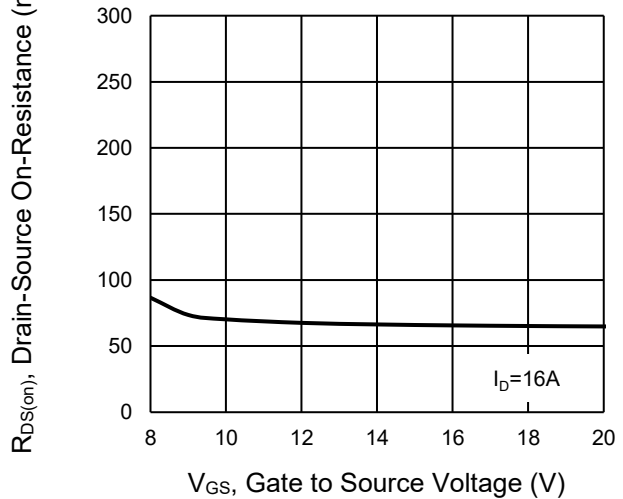
**Gate-Source Voltage vs. Gate Charge**



**On-Resistance vs. Junction Temperature**



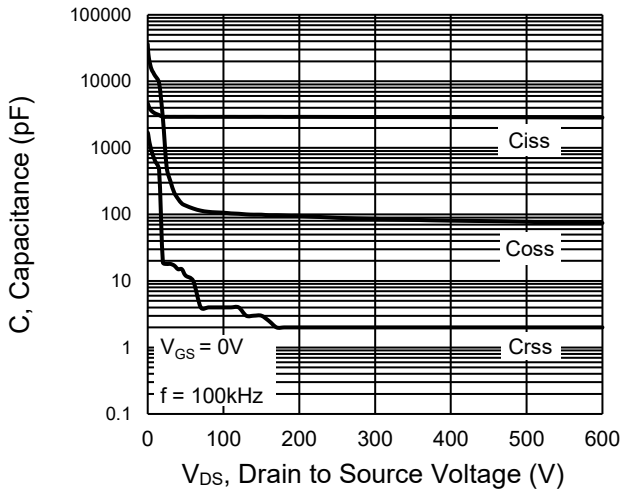
**On-Resistance vs. Gate-Source Voltage**



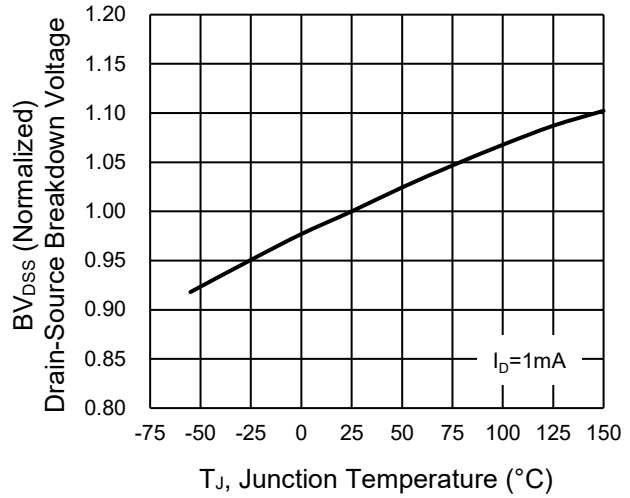
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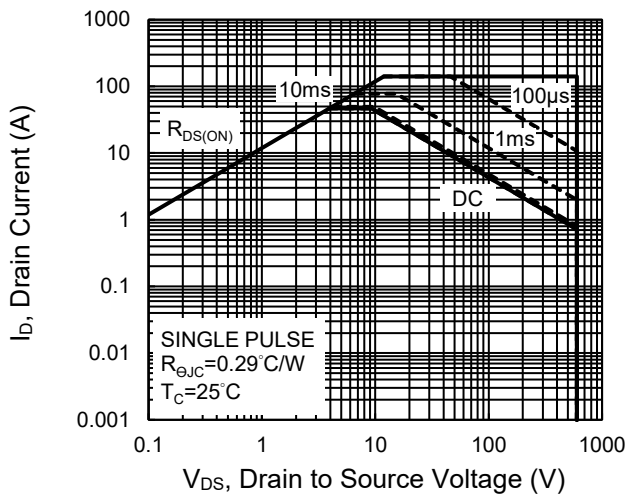
**Capacitance vs. Drain-Source Voltage**



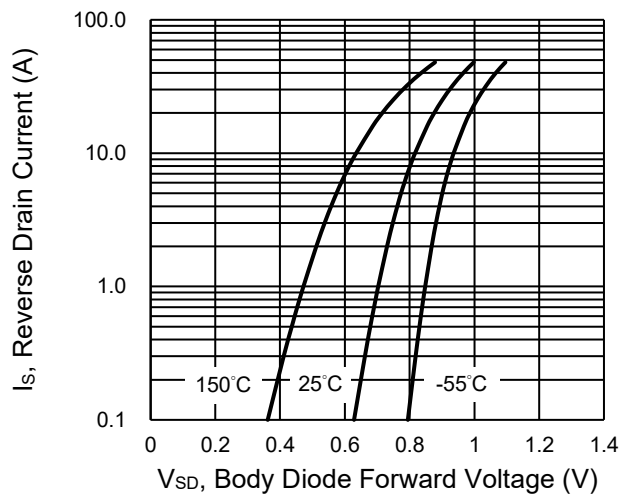
**$BV_{DSS}$  vs. Junction Temperature**



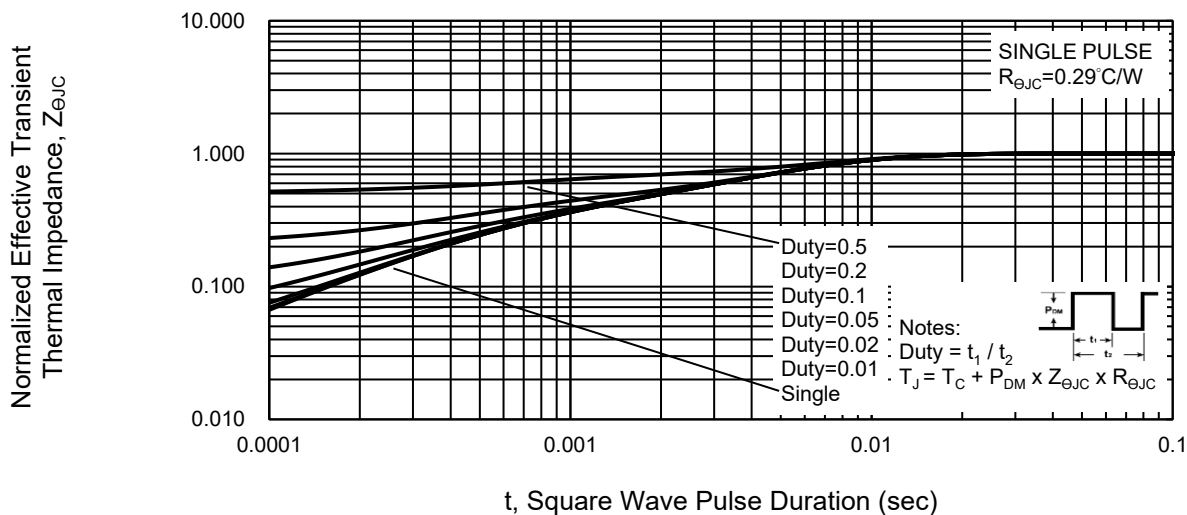
**Maximum Safe Operating Area, Junction-to-Case**



**Source-Drain Diode Forward Current vs. Voltage**



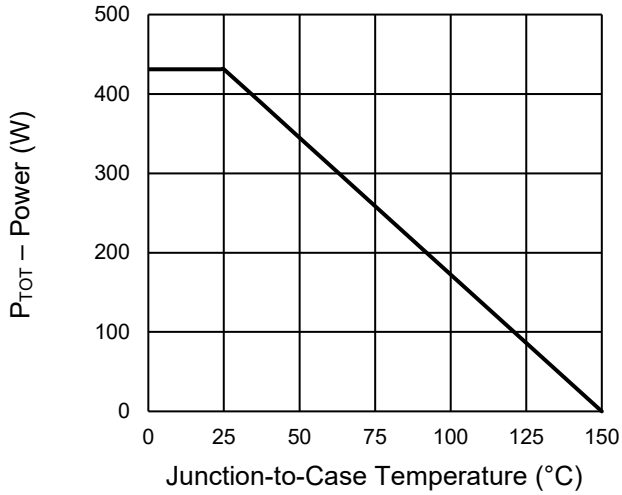
**Normalized Thermal Transient Impedance, Junction-to-Case**



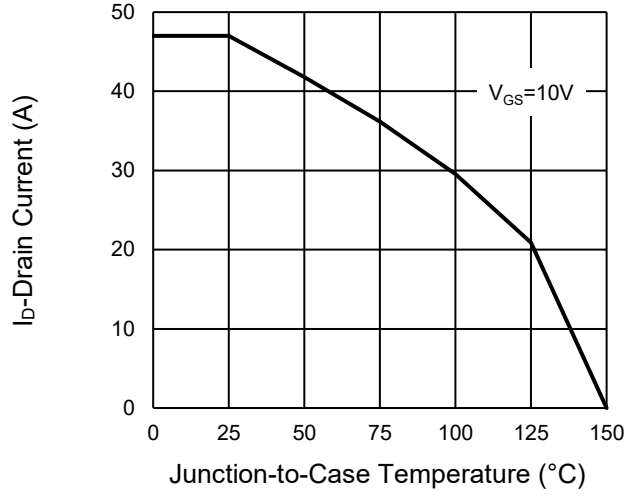
**CHARACTERISTICS CURVES**

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

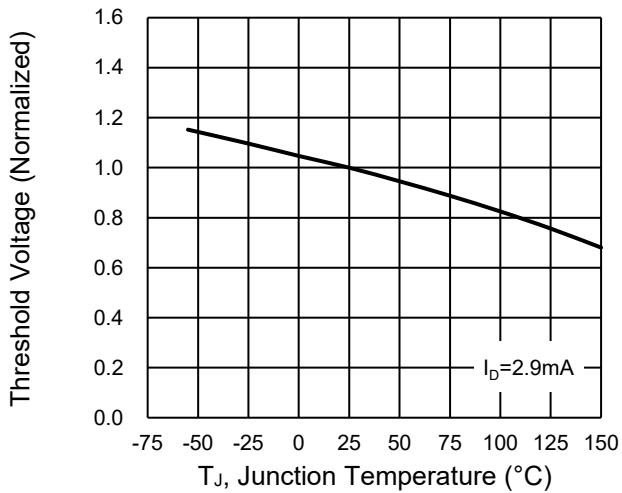
**Power Dissipation**



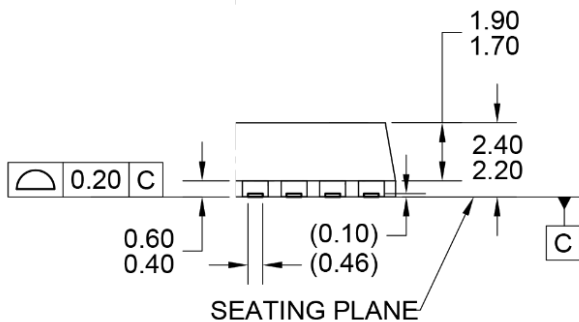
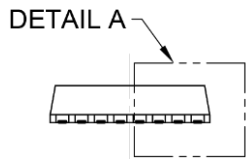
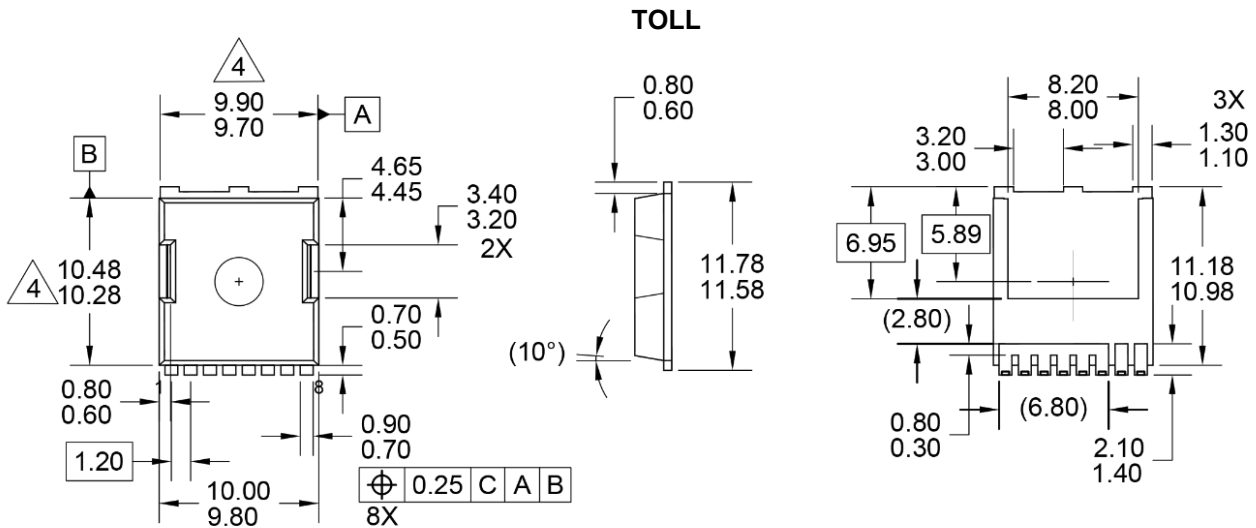
**Drain Current**



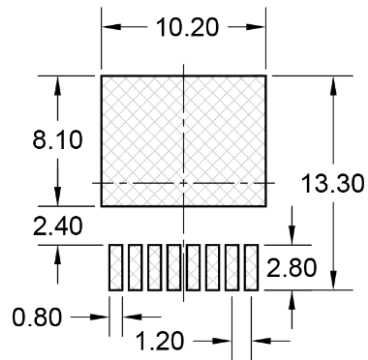
**Normalized gate threshold voltage vs Temperature**



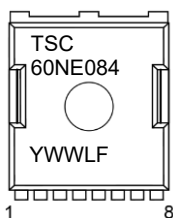
**PACKAGE OUTLINE DIMENSIONS** (Unit: Millimeters)



DETAIL A  
(SCALE 2:1)



**SUGGESTED PAD LAYOUT**



**MARKING DIAGRAM**

- 60NE084 = Device marking
- Y = Year Code
- WW = Week Code (01~52)
- L = Lot Code (1~9,A~Z)
- F = Factory Code

**NOTES: UNLESS OTHERWISE SPECIFIED**

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. THE PACKAGE OUTLINE REFERENCE: JEDEC MO-299B, ISSUE B.
4. MOLDED PLASTIC BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREME OF THE PLASTIC BODY.
5. DWG NO. REF: HQ2SD07-PDFN1012H-130 REV A.

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