N-Channel Power MOSFET

600V, 4A, 0.98Ω

FEATURES

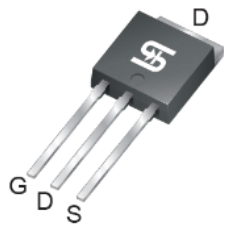
- Super-Junction technology
- High performance due to small figure-of-merit
- High commutation performance
- 100% UIS & Rg tested
- RoHS Compliant
- Halogen-free

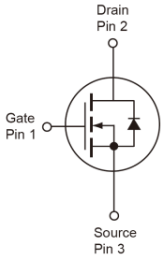
KEY PERFORMANCE PARAMETERS		
PARAMETER	**VALUE**	**UNIT**
V_{DS}	600	V
$R_{DS(on)}$ (max)	0.98	Ω
Q_g	11	nC

APPLICATIONS

- Switching Power Supply
- Lighting

TO-251(IPAK)





ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)				
PARAMETER		**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage		V_{DS}	600	V
Gate-Source Voltage	static	V_{GS}	±20	V
	AC(f>1Hz)		±30	V
Continuous Drain Current	T_C = 25°C	I_D	4	A
Pulsed Drain Current (Note 1)		I_{DM}	12	A
Total Power Dissipation @ T_C = 25°C		P_D	57	W
Single Pulse Avalanche Energy (Note 2)		E_{AS}	91	mJ
Single Pulse Avalanche Current (Note 2)		I_{AS}	1.9	A
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150	°C

THERMAL PERFORMANCE			
PARAMETER	**SYMBOL**	**LIMIT**	**UNIT**
Junction to Case Thermal Resistance	$R_{\Theta JC}$	2.2	°C/W
Junction to Ambient Thermal Resistance	$R_{\Theta JA}$	50	°C/W

Note: $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JA}$ shown below for single device operation on FR-4 PCB with a minimum recommended footprint in still air.

ELECTRICAL SPECIFICATIONS (T_A = 25°C unless otherwise noted)						
PARAMETER	**CONDITIONS**	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
Static (Note 3)						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 1mA	BV_{DSS}	600	--	--	V
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 1mA	$V_{GS(TH)}$	3	4.5	5	V
Gate Body Leakage	V_{GS} = ± 20V, V_{DS} = 0V	I_{GSS}	--	--	±100	nA
Zero Gate Voltage Drain Current	V_{DS} = 600V, V_{GS} = 0V	I_{DSS}	--	--	100	μA
Drain-Source On-State Resistance	V_{GS} = 10V, I_D = 1.5A	$R_{DS(on)}$	--	0.89	0.98	Ω
Dynamic (Note 4)						
Total Gate Charge	V_{DS} = 300V, I_D = 4A, V_{GS} = 10V	Q_g	--	11	--	nC
Gate-Source Charge		Q_{gs}	--	2.9	--	
Gate-Drain Charge		Q_{gd}	--	4.5	--	
Input Capacitance	V_{DS} = 300V, V_{GS} = 0V, f = 1.0MHz	C_{iss}	--	330	--	pF
Output Capacitance		C_{oss}	--	16	--	
Reverse Transfer Capacitance		C_{rss}	--	12	--	
Gate Resistance	f = 1.0MHz	R_g	--	2.7	--	Ω
Switching (Note 5)						
Turn-On Delay Time	V_{DD} = 300V, R_G = 10Ω, I_D = 2A, V_{GS} = 10V	$t_{d(on)}$	--	12	--	ns
Turn-On Rise Time		t_r	--	8.7	--	
Turn-Off Delay Time		$t_{d(off)}$	--	28	--	
Turn-Off Fall Time		t_f	--	17	--	
Source-Drain Diode						
Body-Diode Continuous Forward Current		I_S	--	--	4	A
Body-Diode Pulsed Current (Note 1)		I_{SM}	--	--	12	A
Forward Voltage (Note 3)	I_S = 1.5A, V_{GS} = 0V	V_{SD}	--	--	1.5	V
Reverse Recovery Time (Note 4)	I_S = 4A, dI_F/dt = 100A/μs	t_{rr}	--	239	--	ns
Reverse Recovery Charge (Note 4)		Q_{rr}	--	2.1	--	μC

Notes:

1. Pulse width limited by the maximum junction temperature.
2. L = 50mH, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C
3. Pulse test: PW ≤ 300μs, duty cycle ≤ 2%.
4. Defined by design. Not subject to production test.
5. Switching time is essentially independent of operating temperature.

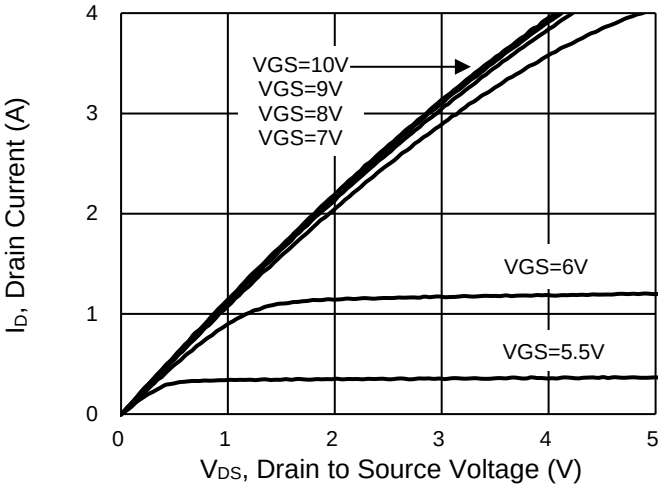
ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TSM60NC980CH C5G	TO-251 (IPAK)	75pcs / Tube

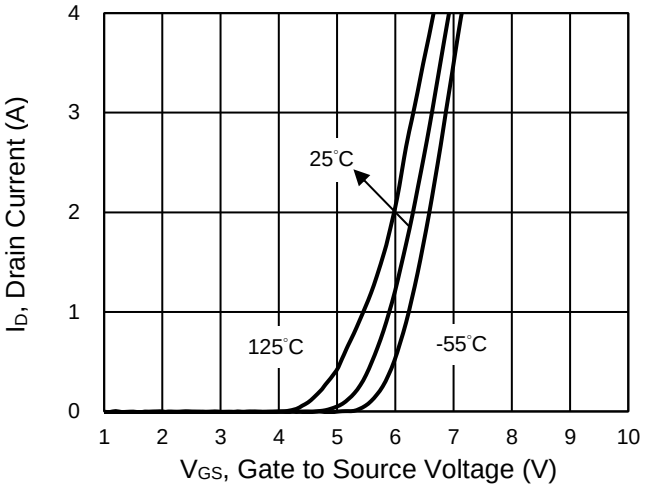
CHARACTERISTICS CURVES

(T_C = 25°C unless otherwise noted)

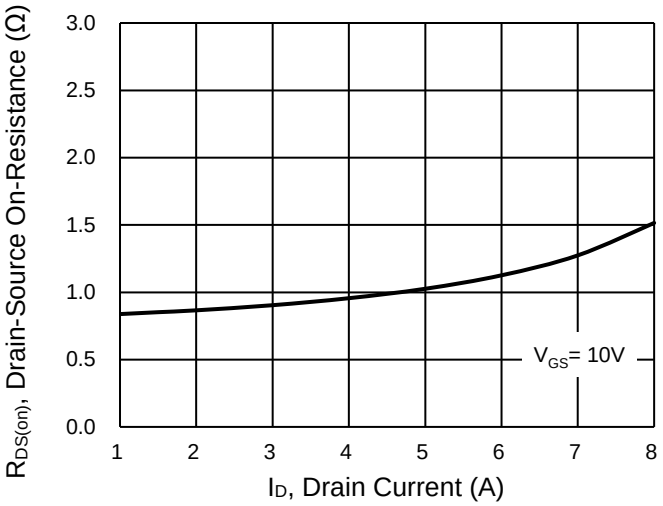
Output Characteristics



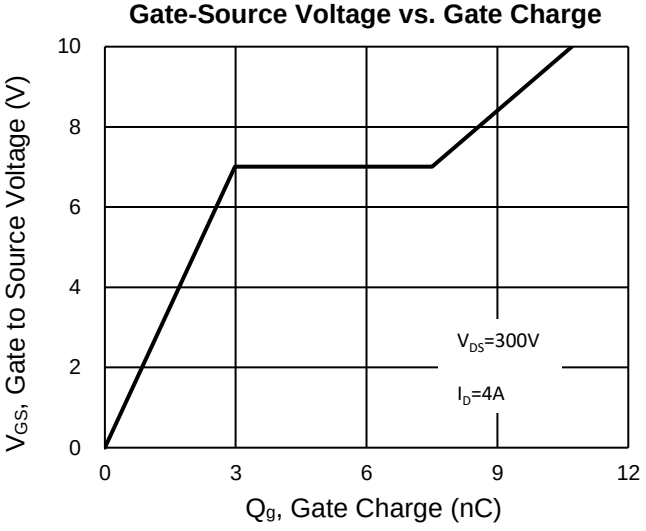
Transfer Characteristics



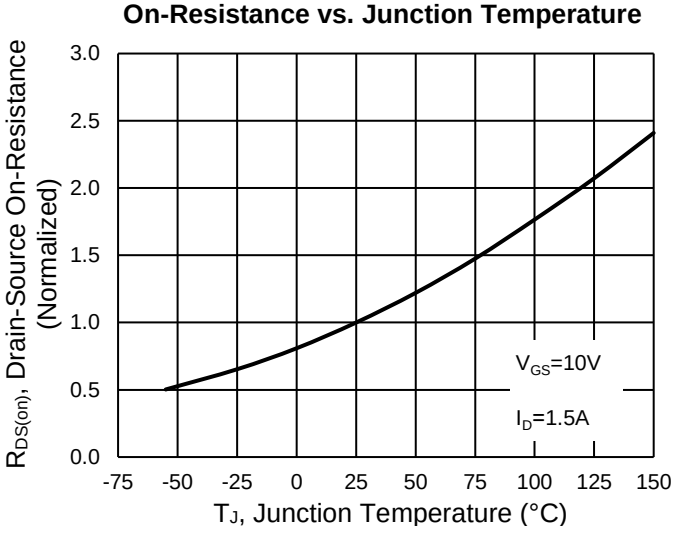
On-Resistance vs. Drain Current



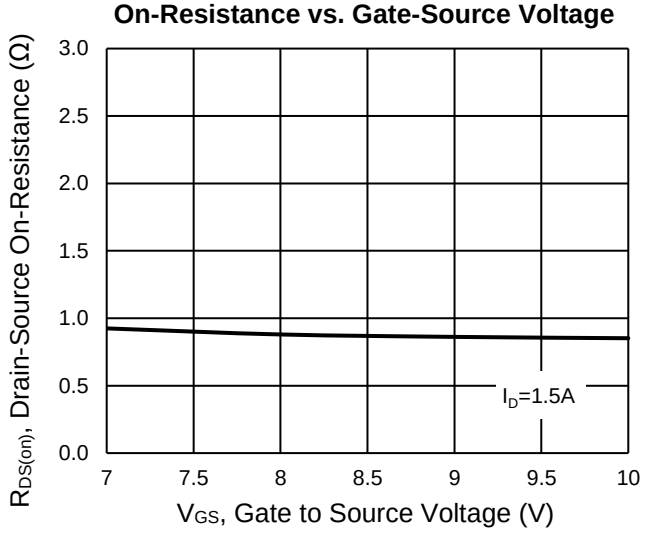
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



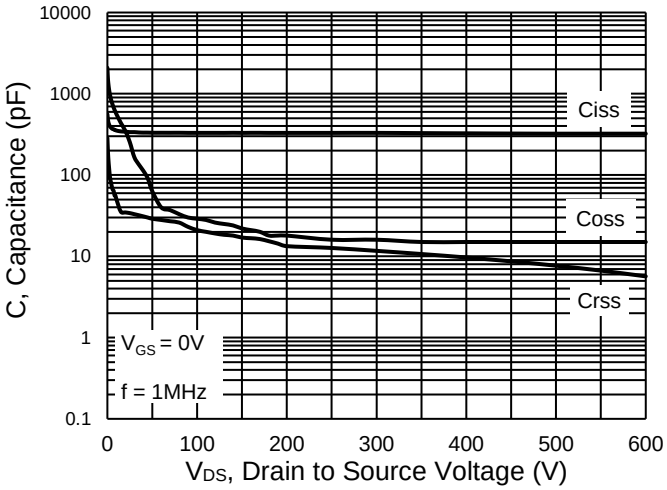
On-Resistance vs. Gate-Source Voltage



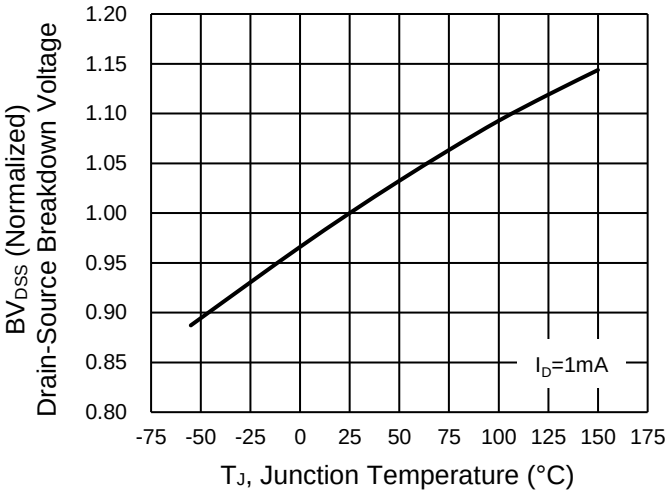
CHARACTERISTICS CURVES

(T_C = 25°C unless otherwise noted)

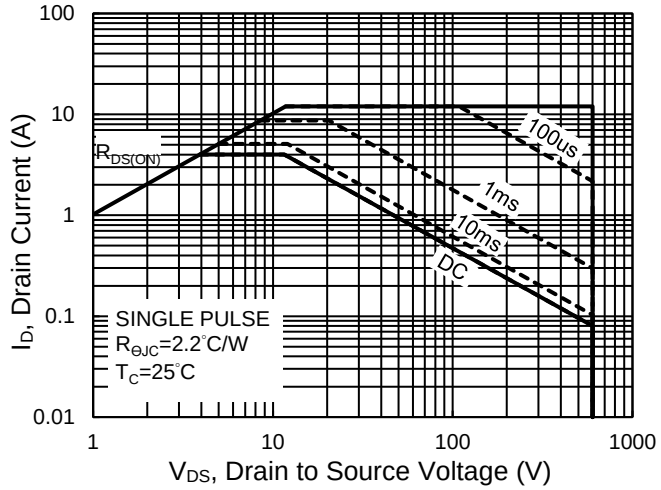
Capacitance vs. Drain-Source Voltage



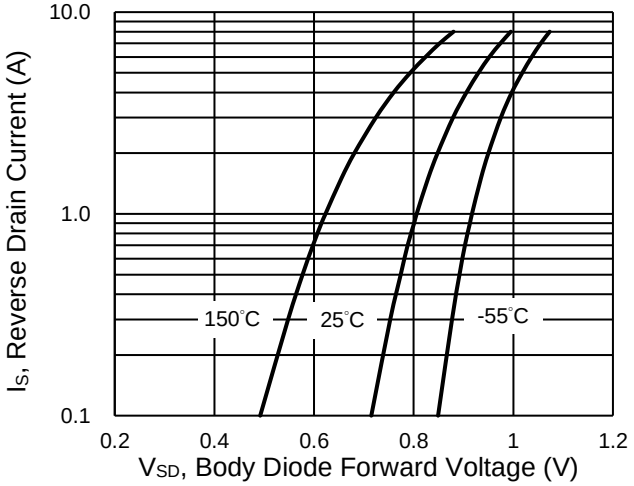
BV_{DSS} vs. Junction Temperature



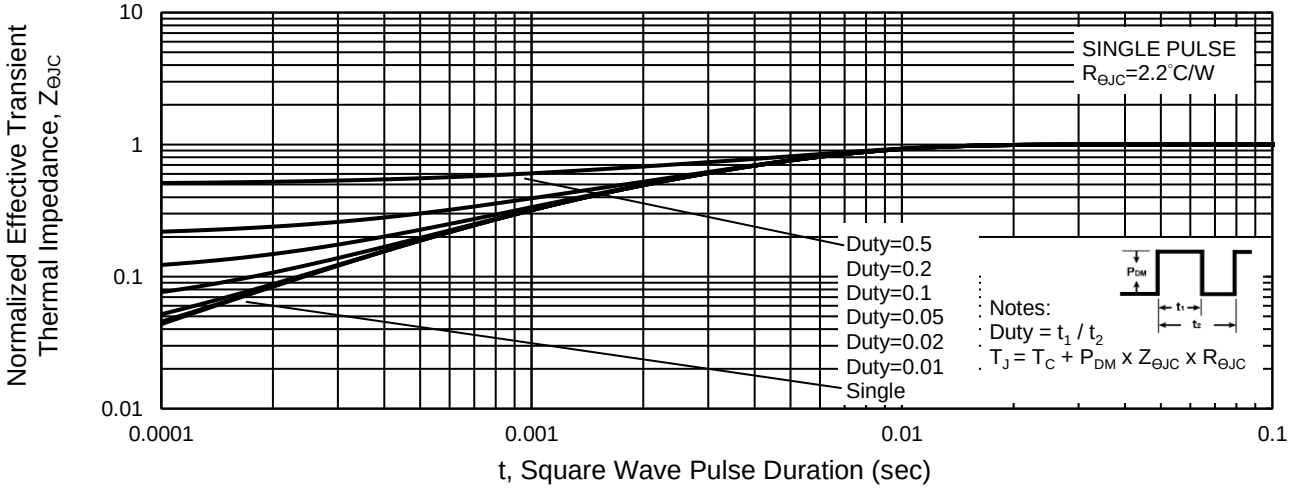
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage



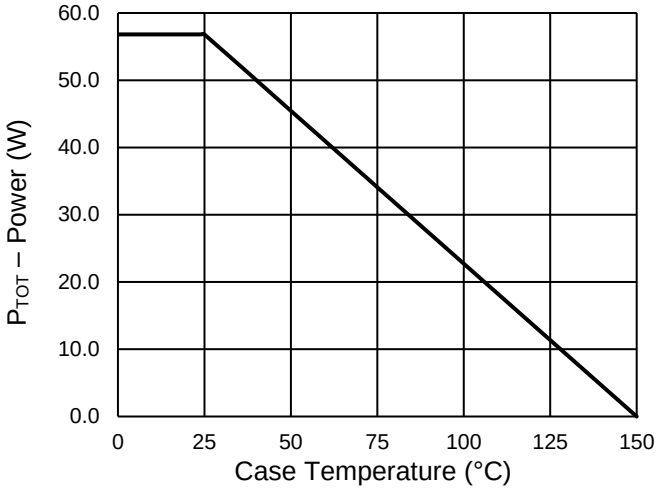
Normalized Thermal Transient Impedance, Junction-to-Case



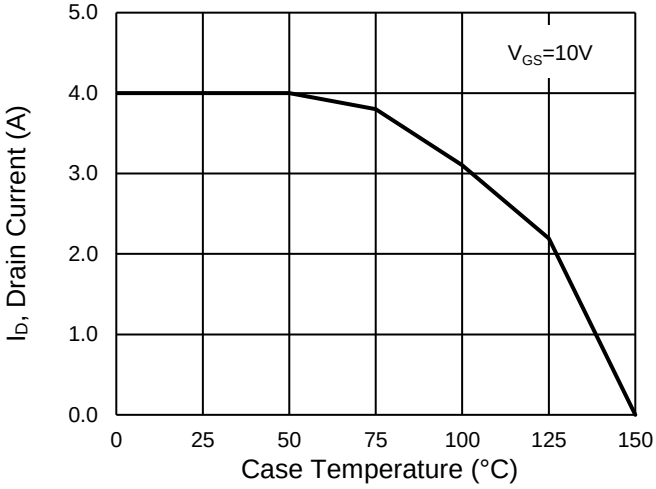
CHARACTERISTICS CURVES

(T_C = 25°C unless otherwise noted)

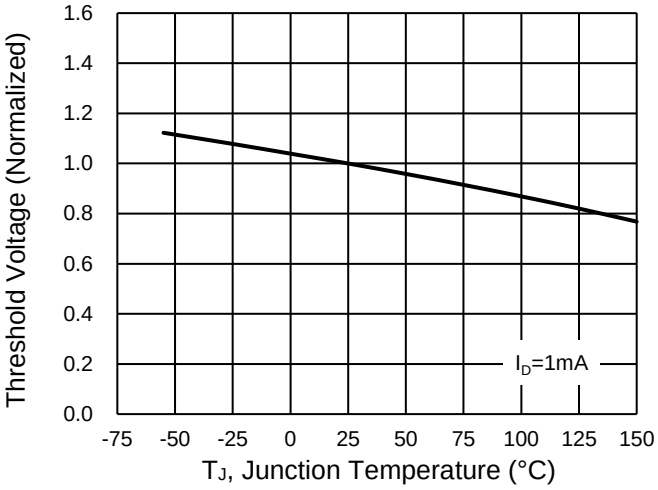
Power Dissipation



Drain Current

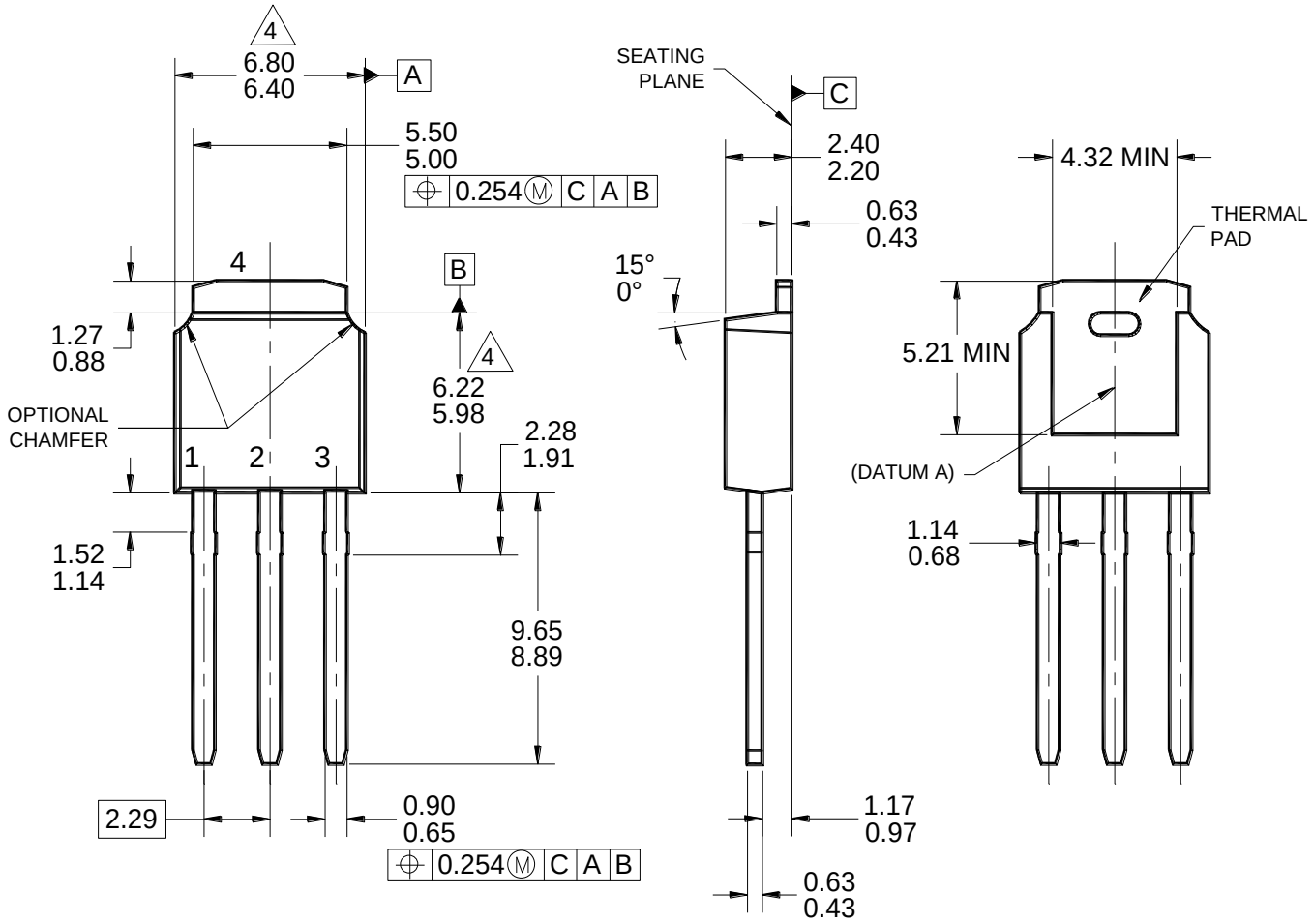


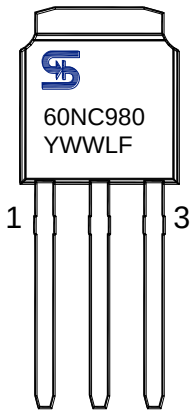
Normalized gate threshold voltage vs Temperature



PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

TO-251





MARKING DIAGRAM

Y	=	YEAR CODE
WW	=	WEEK CODE (01 ~ 52)
L	=	LOT CODE (1~9, A~Z)
F	=	FACTORY CODE

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. THIS CONFORM TO JEDEC PACKAGE REGISTRATION TO-251, VARIATION AA.
4. MOLDED PLASTIC BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
5. DWG NO REF: HQ2SD07-IPAK-005 REV A.

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