

N-Channel Power MOSFET

60V, 35A, 22mΩ

FEATURES

- Low $R_{DS(ON)}$ to minimize conductive losses
- Low gate charge for fast power switching
- 100% UIS and Rg tested.
- 175°C Operating junction temperature
- RoHS Compliant
- Halogen-free

KEY PERFORMANCE PARAMETERS

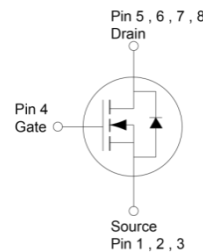
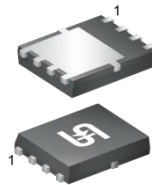
PARAMETER	VALUE	UNIT	
V_{DS}	60	V	
$R_{DS(on)}$ (max)	$V_{GS} = 10V$	22	mΩ
Q_g	21	nC	

APPLICATIONS

- BLDC Motor Control
- Battery Power Management
- DC-DC converter
- Secondary Synchronous Rectification



PDFN56



Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	V_{DS}	60	V	
Gate-Source Voltage	V_{GS}	± 20	V	
Continuous Drain Current (Note 1)	I_D	$T_C = 25^\circ\text{C}$	35	A
		$T_A = 25^\circ\text{C}$	8	
Pulsed Drain Current	I_{DM}	140	A	
Single Pulse Avalanche Current (Note 2)	I_{AS}	15	A	
Single Pulse Avalanche Energy (Note 2)	E_{AS}	33.8	mJ	
Total Power Dissipation	P_D	$T_C = 25^\circ\text{C}$	68	W
		$T_C = 125^\circ\text{C}$	23	
Total Power Dissipation	P_D	$T_A = 25^\circ\text{C}$	3.1	W
		$T_A = 125^\circ\text{C}$	1	
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to +175	$^\circ\text{C}$	

THERMAL PERFORMANCE

PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	2.2	$^\circ\text{C}/\text{W}$
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	48	$^\circ\text{C}/\text{W}$

Notes:

Device on a PCB FR4 with 1 in² (single layer, 2 oz thickness) copper area for drain connection.

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV_{DSS}	60	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	$V_{GS(TH)}$	2	3.3	4	V
Gate-Source Leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$	I_{GSS}	--	--	± 100	nA
Drain-Source Leakage Current	$V_{DS} = 60V, V_{GS} = 0V$	I_{DSS}	--	--	1	μA
	$V_{DS} = 60V, V_{GS} = 0V$ $T_J = 125^\circ\text{C}$		--	--	100	
Drain-Source On-State Resistance (Note 3)	$V_{GS} = 10V, I_D = 8A$	$R_{DS(on)}$	--	19	22	m Ω
Forward Transconductance (Note 3)	$V_{DS} = 10V, I_D = 8A$	g_{fs}	--	35	--	S
Dynamic (Note 4)						
Total Gate Charge	$V_{DS} = 30V, I_D = 8A,$ $V_{GS} = 10V$	Q_g	--	21	--	nC
Gate-Source Charge		Q_{gs}	--	6.6	--	
Gate-Drain Charge		Q_{gd}	--	4.6	--	
Input Capacitance	$V_{DS} = 30V, V_{GS} = 0V,$ $f = 1.0\text{MHz}$	C_{iss}	--	1420	--	pF
Output Capacitance		C_{oss}	--	84	--	
Reverse Transfer Capacitance		C_{rss}	--	52	--	
Gate Resistance	$f = 1.0\text{MHz}$	R_g	0.6	1.8	4	Ω
Switching (Note 4)						
Turn-On Delay Time	$V_{DD} = 30V, R_G = 2\Omega,$ $I_D = 8A, V_{GS} = 10V$	$t_{d(on)}$	--	9.6	--	ns
Turn-On Rise Time		t_r	--	20	--	
Turn-Off Delay Time		$t_{d(off)}$	--	17	--	
Turn-Off Fall Time		t_f	--	17	--	
Source-Drain Diode						
Forward Voltage (Note 3)	$I_S = 8A, V_{GS} = 0V$	V_{SD}	--	--	1.2	V
Reverse Recovery Time	$I_S = 8A,$ $di/dt = 100A/\mu s$	t_{rr}	--	18	--	ns
Reverse Recovery Charge		Q_{rr}	--	14	--	nC

Notes:

1. Silicon limited current only.
2. $L = 0.3\text{mH}, V_{GS} = 10V, V_{DD} = 30V, R_G = 25\Omega,$ Starting $T_J = 25^\circ\text{C}$.
3. Pulse test: Pulse Width $\leq 300\mu s,$ duty cycle $\leq 2\%$.
4. Switching time is essentially independent of operating temperature.

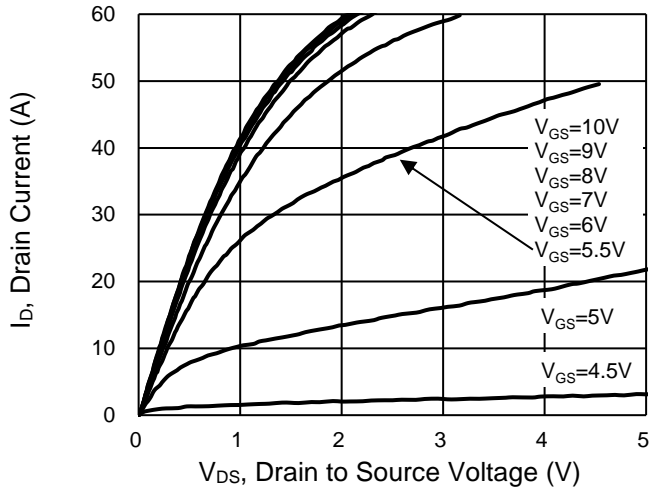
ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TSM220NB06CR RLG	PDFN56	2500pcs / 13" Reel

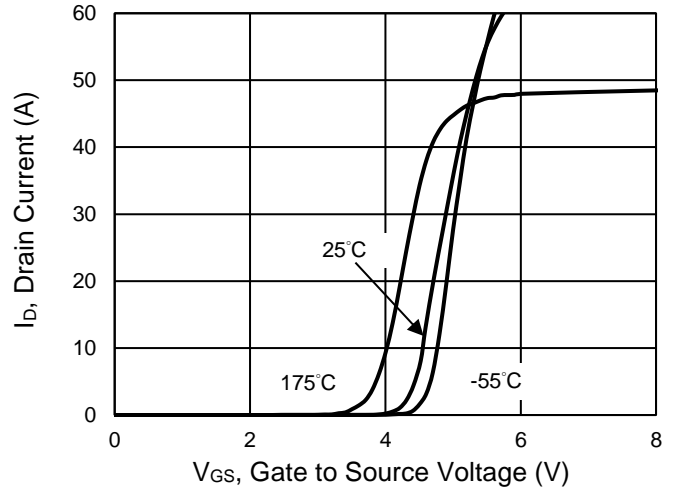
CHARACTERISTICS CURVES (N-Channel)

($T_A = 25^\circ\text{C}$ unless otherwise noted)

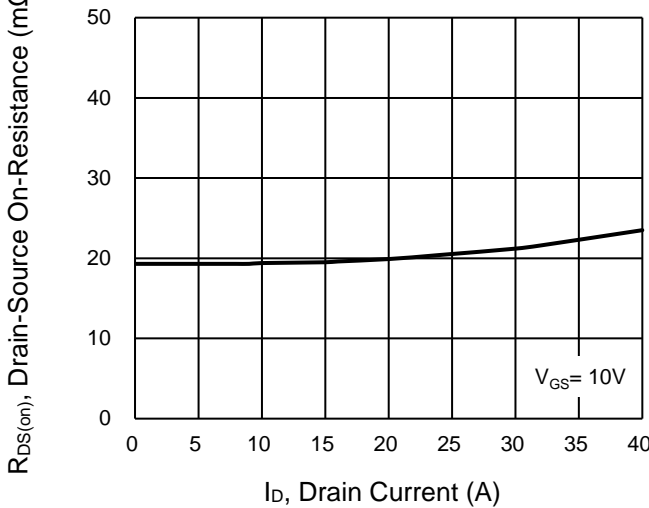
Output Characteristics



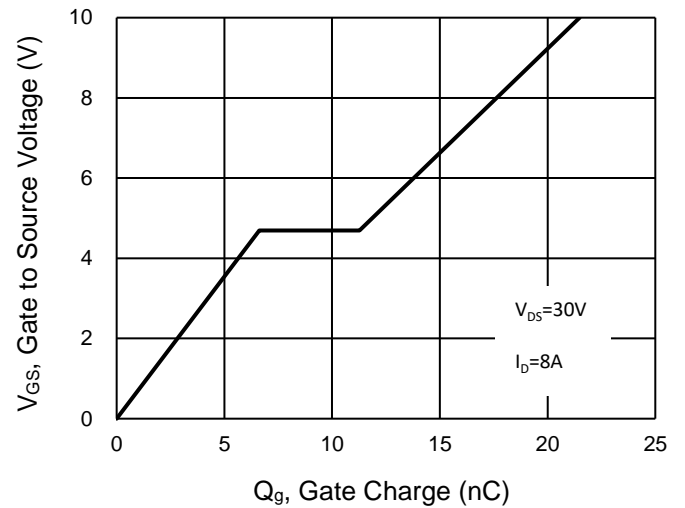
Transfer Characteristics



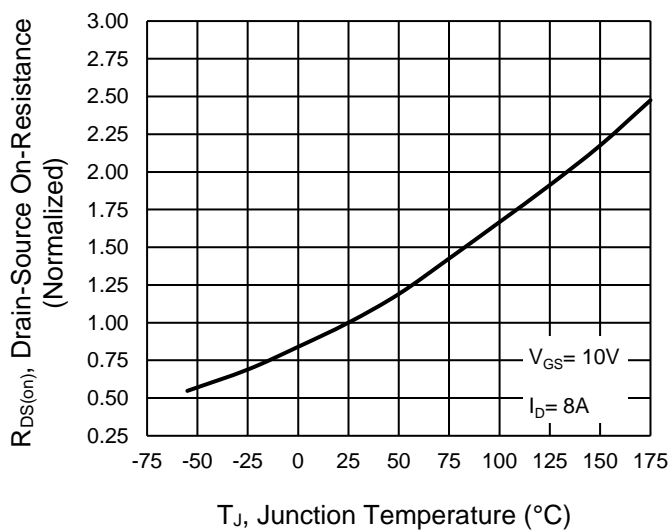
On-Resistance vs. Drain Current



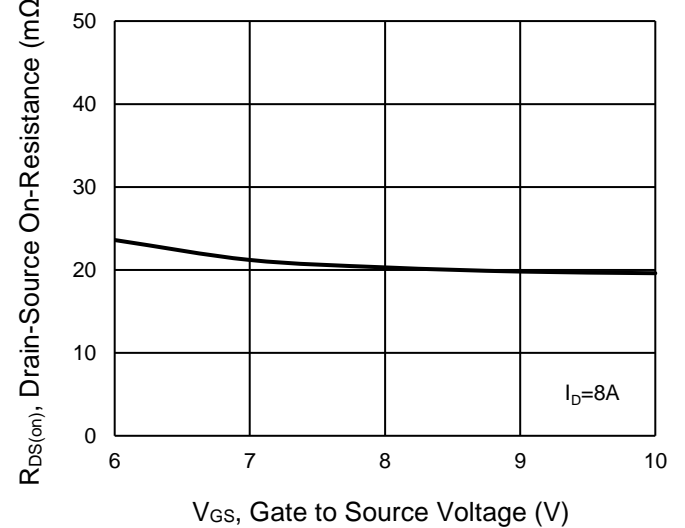
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature

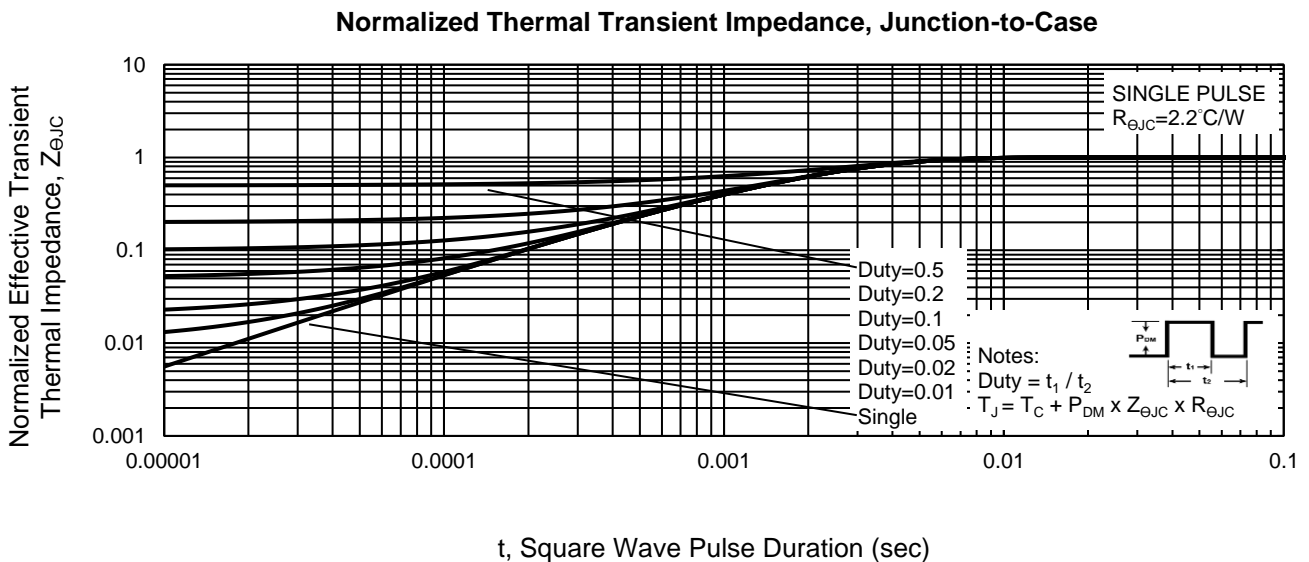
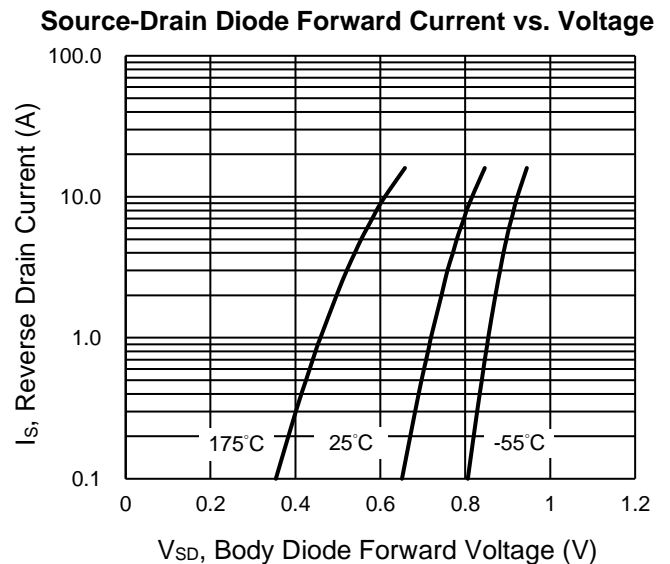
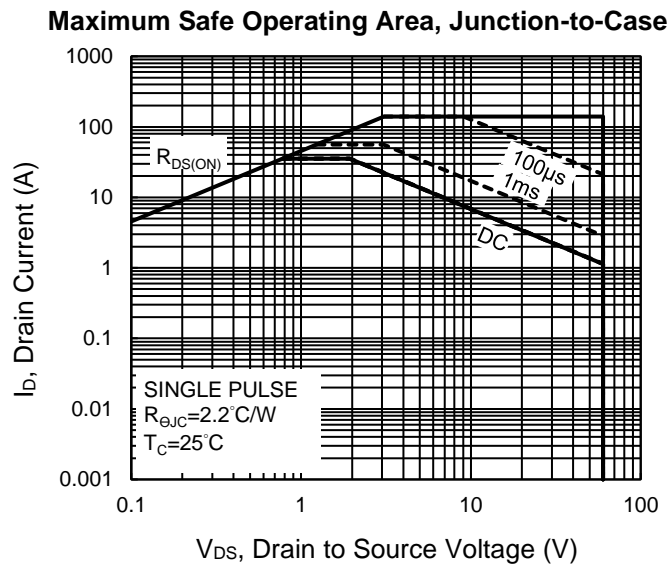
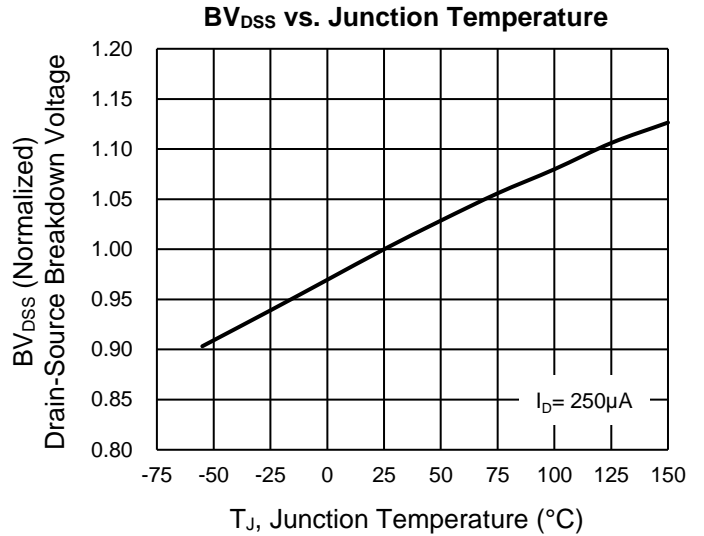
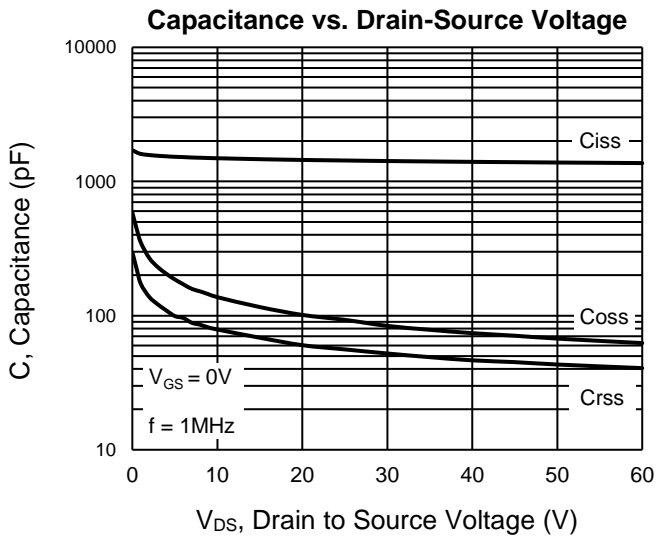


On-Resistance vs. Gate-Source Voltage



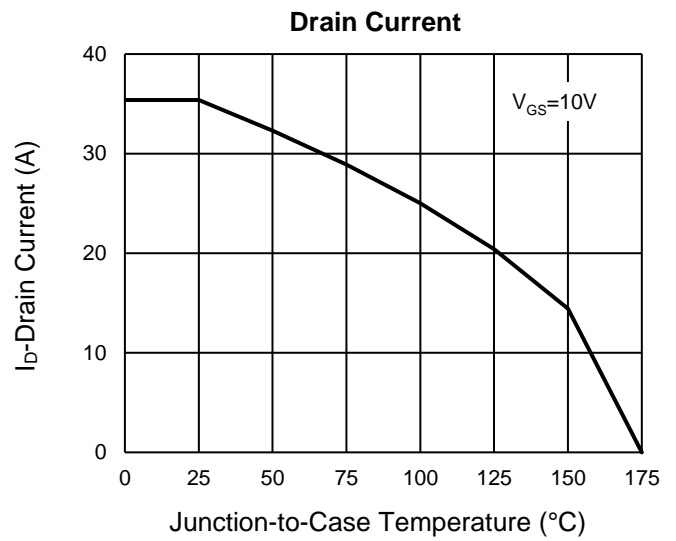
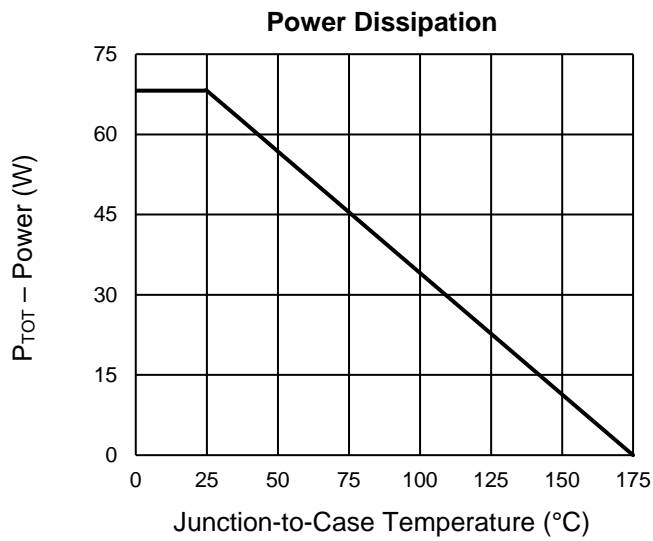
CHARACTERISTICS CURVES (N-Channel)

($T_A = 25^\circ\text{C}$ unless otherwise noted)

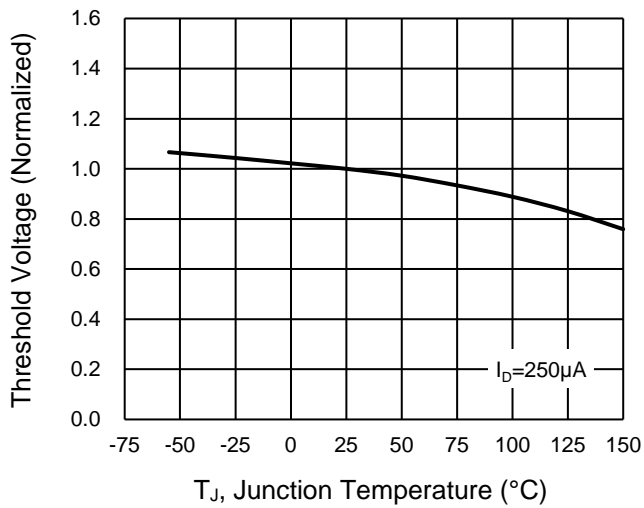


CHARACTERISTICS CURVES (N-Channel)

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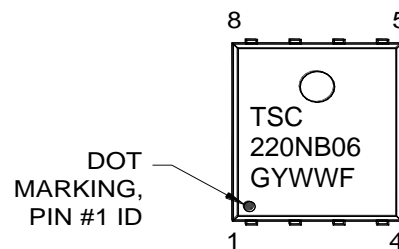
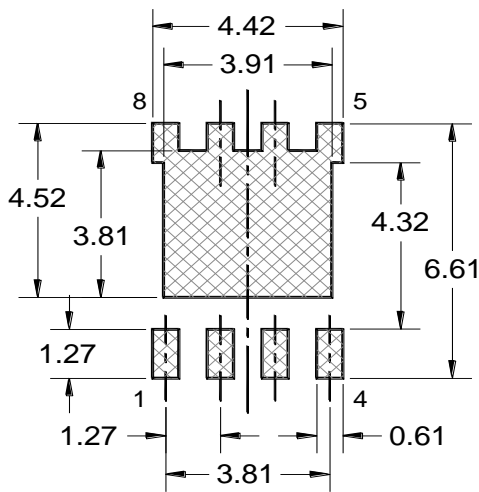
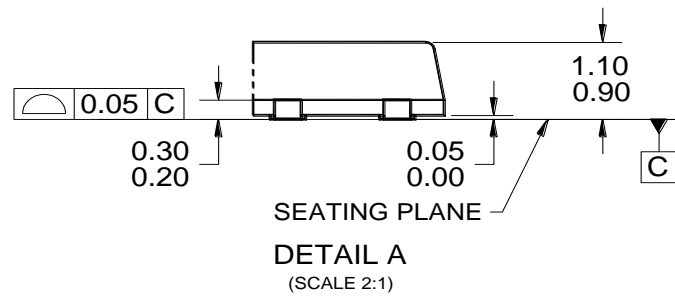
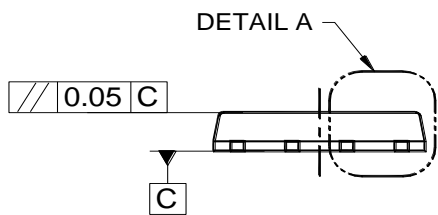
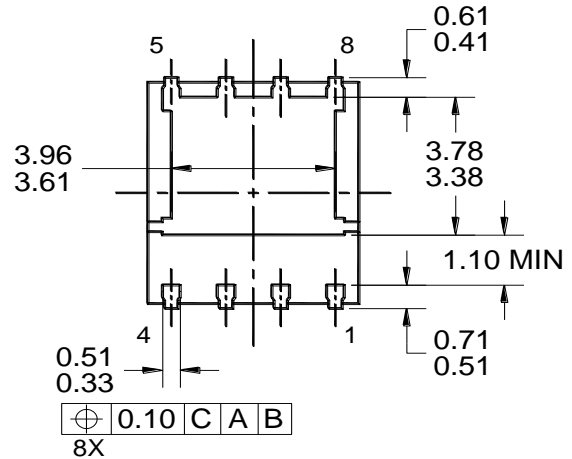
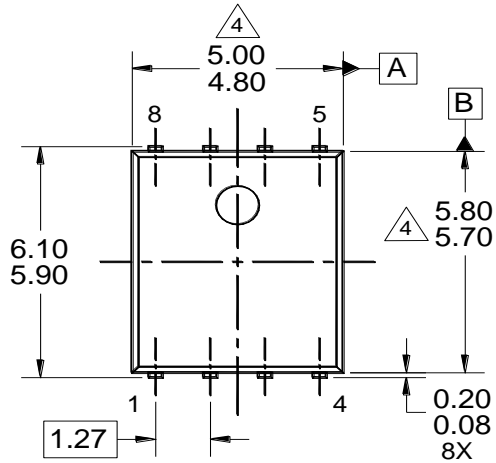


Normalized gate threshold voltage vs Temperature



PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

PDFN56



SUGGESTED PAD LAYOUT
(REFERENCE ONLY)

MARKING DIAGRAM

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PACKAGE OUTLINE REFERENCE: JEITA ED-7500B, EIAJ SC-111BB.
4. MOLDED PLASTIC BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
5. DWG NO REF: HQ2SD07-PDFN56-021 REV A.

- G = Halogen Free
- Y = Year Code
- WW = Week Code (01~52)
- F = Factory Code

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