

P-Channel Power MOSFET

-30V, -64A, 8.5mΩ

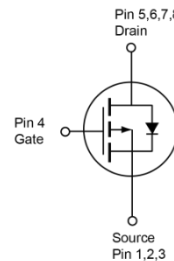
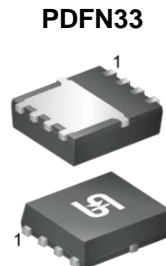
FEATURES

- Low $R_{DS(on)}$ to minimize conductive losses
- Low gate charge for fast power switching
- 100% UIS and R_g tested
- RoHS Compliant
- Halogen-free

APPLICATIONS

- DC-DC converters
- Battery power management
- Load switch
- BLDC motor drives

KEY PERFORMANCE PARAMETERS		
PARAMETER	VALUE	UNIT
V_{DS}	-30	V
$R_{DS(on)}$ (max)	$V_{GS} = -10V$	8.5
	$V_{GS} = -4.5V$	14
Q_g	27	nC



Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current, Silicon limited	$T_C = 25^\circ\text{C}$	I_D	-64
Continuous Drain Current (Note 1)	$T_C = 25^\circ\text{C}$	I_D	-23
	$T_A = 25^\circ\text{C}$		-14
Pulsed Drain Current	I_{DM}	-92	A
Single Pulse Avalanche Current (Note 2)	I_{AS}	25.4	A
Single Pulse Avalanche Energy (Note 2)	E_{AS}	97.2	mJ
Total Power Dissipation	P_D	$T_C = 25^\circ\text{C}$	50
		$T_C = 125^\circ\text{C}$	10
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150	$^\circ\text{C}$

THERMAL PERFORMANCE			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	2.5	$^\circ\text{C/W}$
Junction to Ambient Thermal Resistance (Note 3)	$R_{\theta JA}$	53	$^\circ\text{C/W}$

Notes:

1. Package current limit.
2. $L = 0.3\text{mH}$, $V_{GS} = -10V$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$.
3. Device on a PCB FR4 with 1 in^2 (single layer, 2 oz thickness) copper area for drain connection.

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static (Note 4)						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = -250\mu A$	BV_{DSS}	-30	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\mu A$	$V_{GS(TH)}$	-1.2	-1.6	-2.5	V
Gate Body Leakage	$V_{GS} = \pm 20V, V_{DS} = 0V$	I_{GSS}	--	--	± 100	nA
Zero Gate Voltage Drain Current	$V_{GS} = 0V, V_{DS} = -30V$	I_{DSS}	--	--	-1	μA
	$V_{GS} = 0V, V_{DS} = -30V$ $T_J = 125^\circ\text{C}$		--	--	-100	
Drain-Source On-State Resistance	$V_{GS} = -10V, I_D = -14A$	$R_{DS(on)}$	--	7.8	8.5	m Ω
	$V_{GS} = -4.5V, I_D = -14A$		--	11	14	
Forward Transconductance	$V_{DS} = -5V, I_D = -14A$	g_{fs}	--	42	--	S
Dynamic (Note 5)						
Total Gate Charge	$V_{DS} = -15V, I_D = -14A,$ $V_{GS} = -4.5V$	Q_g	--	27	--	nC
Total Gate Charge	$V_{DS} = -15V, I_D = -14A,$ $V_{GS} = -10V$	Q_g	--	55	--	
Gate-Source Charge		Q_{gs}	--	9.2	--	
Gate-Drain Charge		Q_{gd}	--	10	--	
Input Capacitance	$V_{DS} = -15V, V_{GS} = 0V,$ $f = 1.0\text{MHz}$	C_{iss}	--	3289	--	pF
Output Capacitance		C_{oss}	--	415	--	
Reverse Transfer Capacitance		C_{rss}	--	280	--	
Gate Resistance	$f = 1.0\text{MHz}$	R_g	1.6	5.4	12	Ω
Switching (Note 6)						
Turn-On Delay Time	$V_{GS} = -10V, V_{DS} = -15V,$ $I_D = -14A, R_G = 2\Omega,$	$t_{d(on)}$	--	8.8	--	ns
Turn-On Rise Time		t_r	--	43	--	
Turn-Off Delay Time		$t_{d(off)}$	--	66	--	
Turn-Off Fall Time		t_f	--	41	--	
Source-Drain Diode						
Forward Voltage (Note 4)	$I_S = -14A, V_{GS} = 0V$	V_{SD}	--	--	-1	V
Reverse Recovery Time	$I_S = -14A,$ $dI/dt = 100A/\mu s$	t_{rr}	--	25	--	ns
Reverse Recovery Charge		Q_{rr}	--	13	--	nC

Notes:

- Pulse test: Pulse Width $\leq 300\mu s$, duty cycle $\leq 2\%$.
- Defined by design. Not subject to production test.
- Switching time is essentially independent of operating temperature.

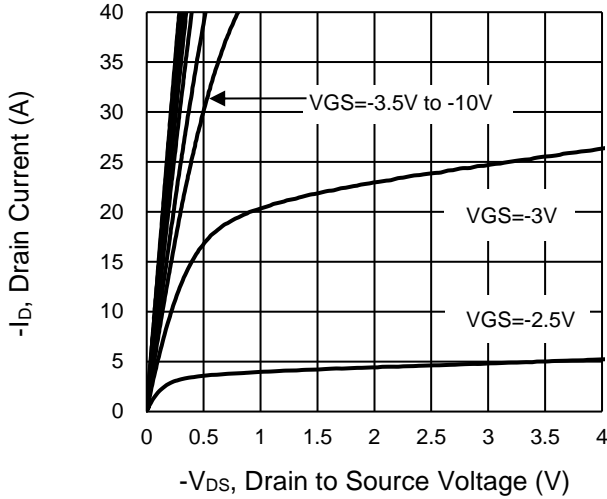
ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TSM085P03CV RGG	PDFN33	5,000pcs / 13" Reel

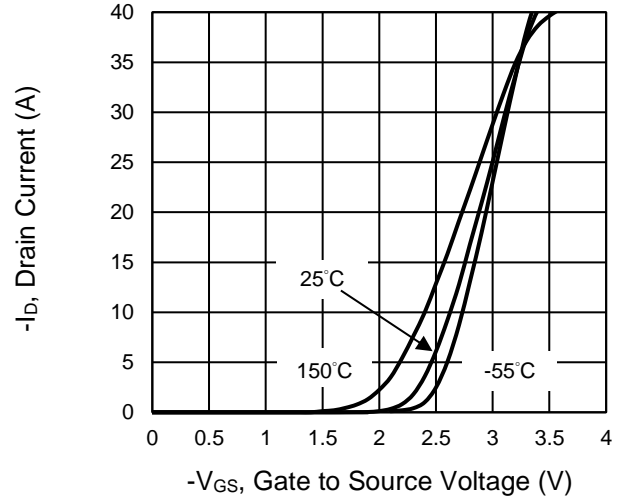
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

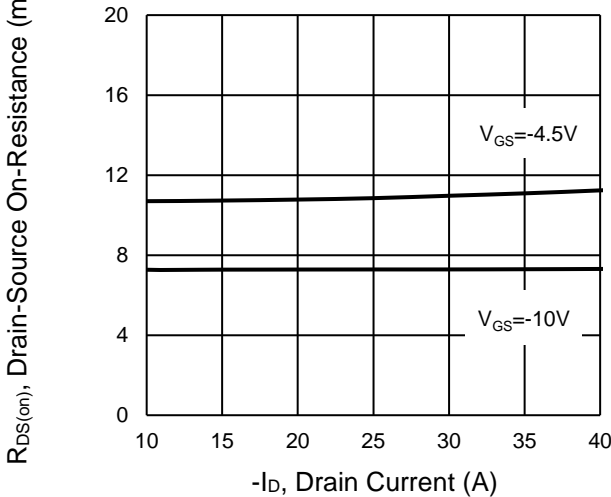
Output Characteristics



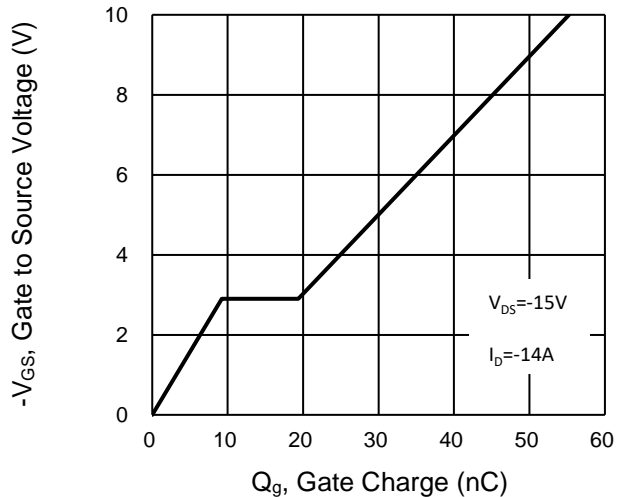
Transfer Characteristics



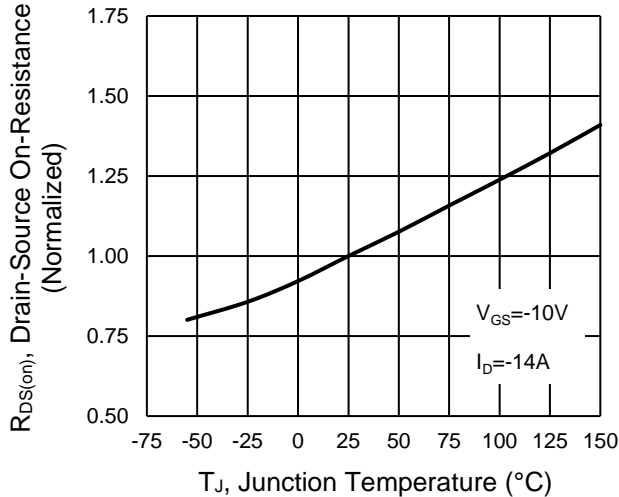
On-Resistance vs. Drain Current



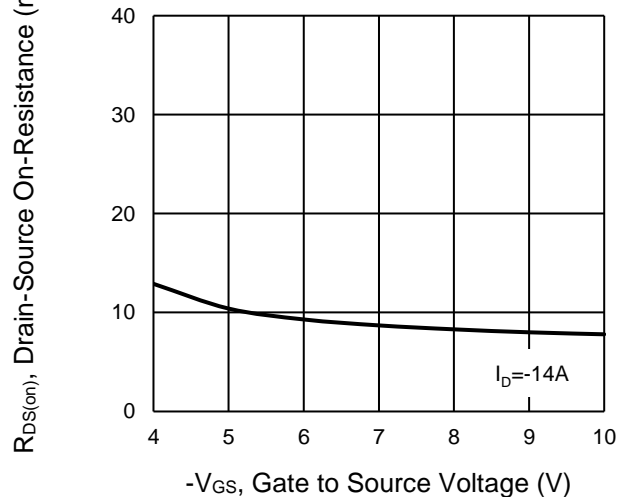
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



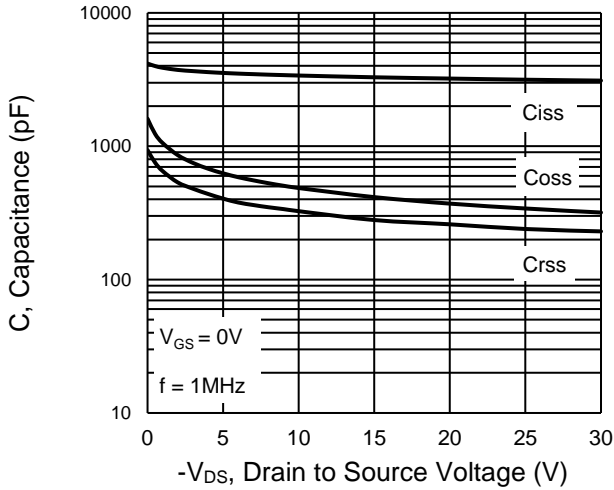
On-Resistance vs. Gate-Source Voltage



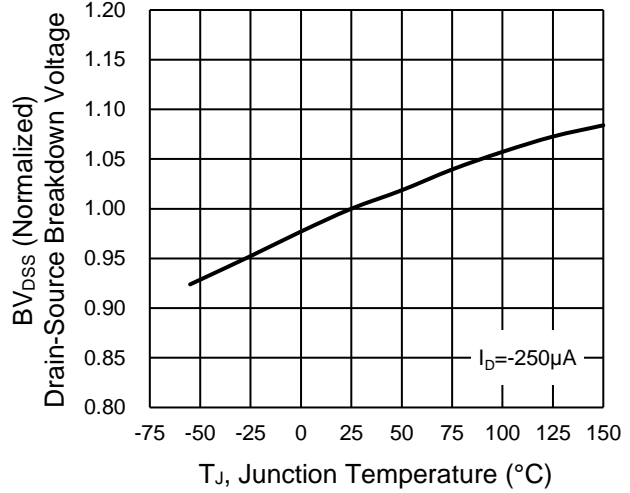
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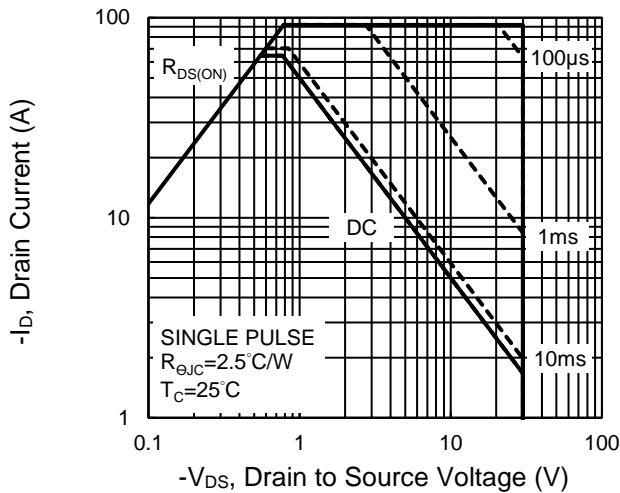
Capacitance vs. Drain-Source Voltage



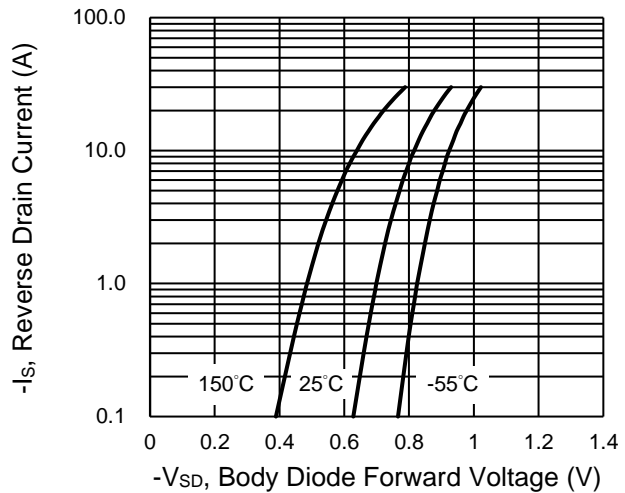
BV_{DSS} vs. Junction Temperature



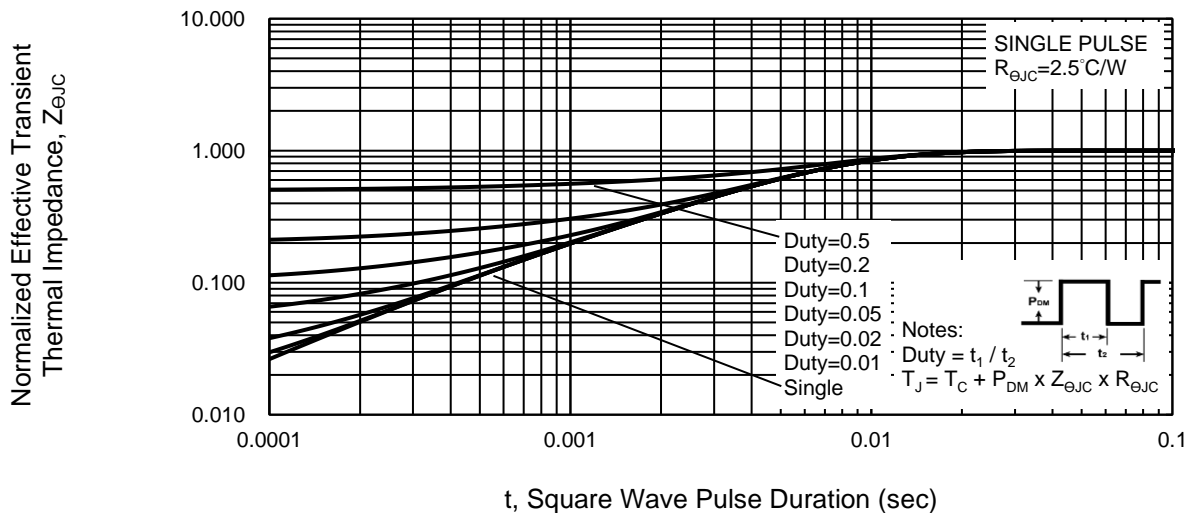
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage



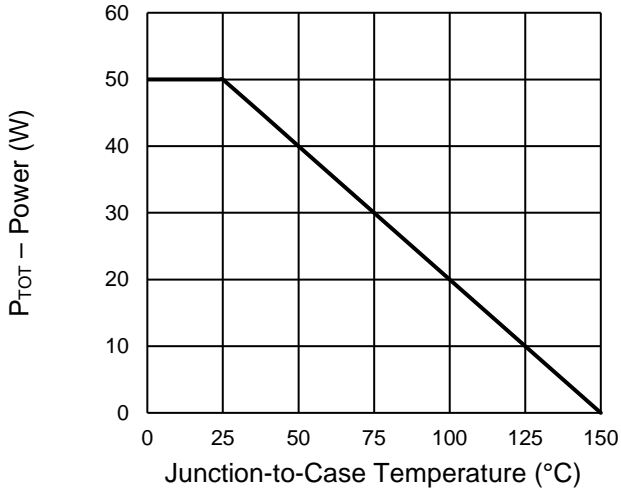
Normalized Thermal Transient Impedance, Junction-to-Case



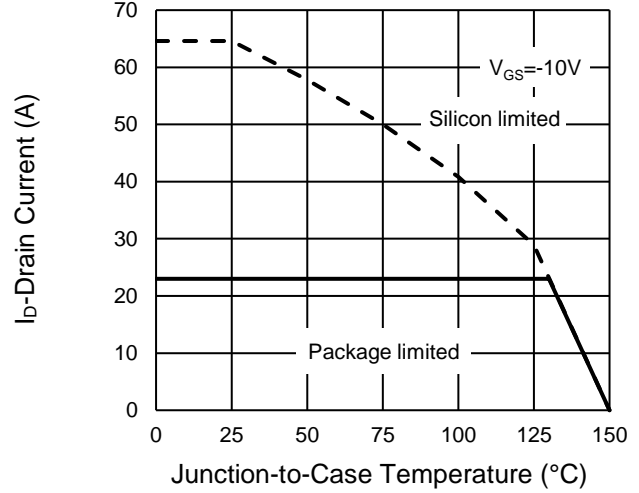
CHARACTERISTICS CURVES

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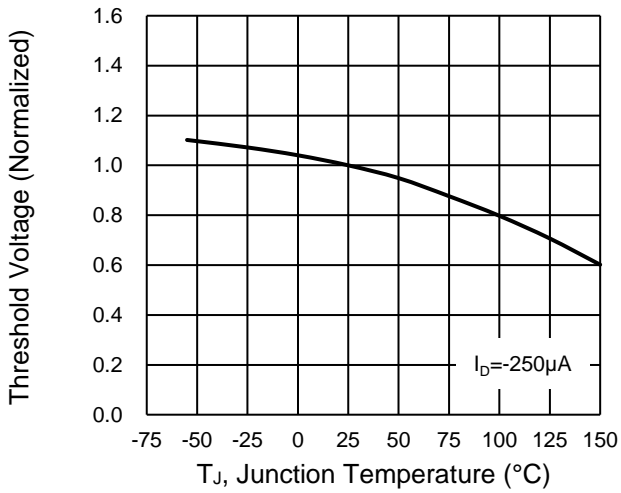
Power Dissipation



Drain Current

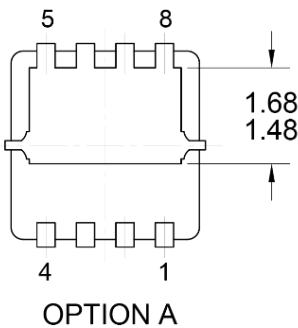
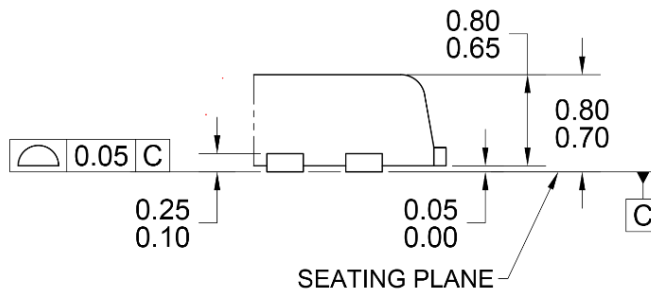
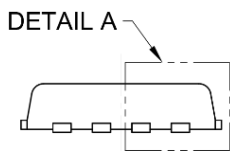
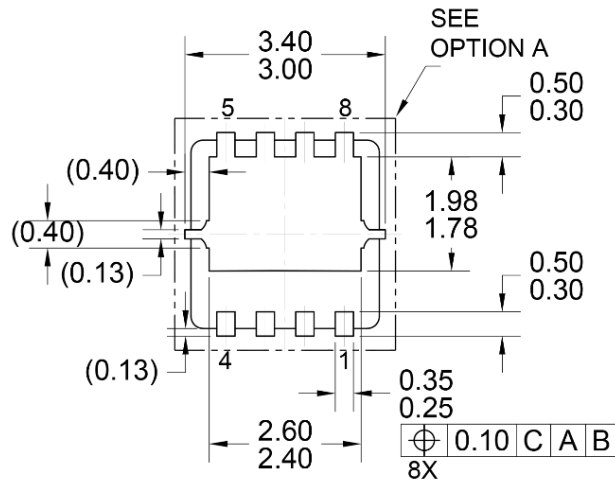
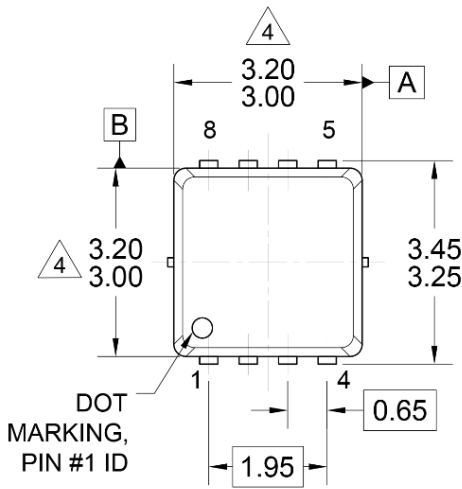


Normalized gate threshold voltage vs Temperature

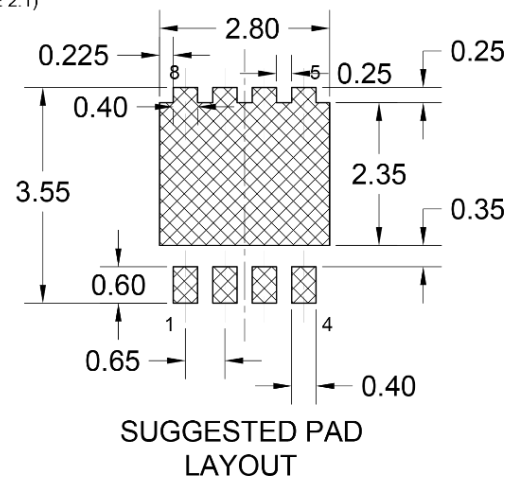


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

PDFN33



DETAIL A
(SCALE 2:1)



MARKING DIAGRAM

- 085P03 = Device marking
- Y = Year Code
- M = Month Code for Halogen Free Product
(O=Jan, P=Feb, Q=Mar, R=Apl, S=May, T=Jun, U=Jul, V=Aug, W=Sep, X=Oct, Y=Nov, Z=Dec)
- L = Lot Code

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PACKAGE OUTLINE REFERENCE: EIAJ SC-119.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
5. DWG NO REF: HQ2SD07-PDFN33-020 REV A.

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