

PerFET™ Power Transistor

FEATURES

- Ultra-low On-resistance
- Wettable Flank leads for Enhanced AOI
- 100% UIS and Rg tested
- 175°C Operating Junction Temperature
- RoHS Compliant
- Halogen-Free according to IEC 61249-2-21

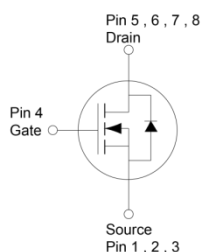
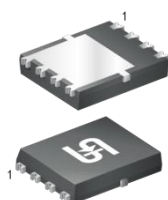
PRODUCT SUMMARY			
PARAMETER	VALUE	UNIT	
V_{DS}	40	V	
$R_{DS(on)}$ (max)	$V_{GS} = 10V$	2.5	mΩ
	$V_{GS} = 7V$	3	
Q_g	$V_{GS} = 10V$	59	nC

APPLICATIONS

- DC-DC Converters
- Solenoid and Motor Drivers
- Load Switch



PDFN56U



Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current, Silicon limited	$T_C = 25^\circ\text{C}$	I_D	174	A
Continuous Drain Current (Note 1)	$T_C = 25^\circ\text{C}$	I_D	100	A
	$T_C = 100^\circ\text{C}$		100	
	$T_A = 25^\circ\text{C}$		26	
Pulsed Drain Current		I_{DM}	400	A
Single Pulse Avalanche Current (Note 2)		I_{AS}	34.9	A
Single Pulse Avalanche Energy (Note 2)		E_{AS}	182.3	mJ
Total Power Dissipation	$T_C = 25^\circ\text{C}$	P_D	136	W
	$T_C = 125^\circ\text{C}$		45	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +175	$^\circ\text{C}$

THERMAL RESISTANCE			
PARAMETER	SYMBOL	MAXIMUM	UNIT
Thermal Resistance – Junction to Case	$R_{\theta JC}$	1.1	$^\circ\text{C/W}$
Thermal Resistance – Junction to Ambient	$R_{\theta JA}$	50	$^\circ\text{C/W}$

Note: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{V}, I_D = 1\text{mA}$	BV_{DSS}	40	--	--	V
Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	$V_{GS(TH)}$	2.4	3	3.6	V
Gate-Source Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$	I_{GSS}	--	--	± 100	nA
Drain-Source Leakage Current	$V_{GS} = 0\text{V}, V_{DS} = 40\text{V}$	I_{DSS}	--	--	1	μA
	$V_{GS} = 0\text{V}, V_{DS} = 40\text{V}$ $T_J = 125^\circ\text{C}$		--	--	100	
Drain-Source On-State Resistance (Note 3)	$V_{GS} = 10\text{V}, I_D = 50\text{A}$	$R_{DS(on)}$	--	1.8	2.5	m Ω
	$V_{GS} = 7\text{V}, I_D = 50\text{A}$		--	2	3	
Forward Transconductance (Note 3)	$V_{DS} = 10\text{V}, I_D = 12.5\text{A}$	g_{fs}	--	83.3	--	s
Dynamic						
Total Gate Charge	$V_{GS} = 7\text{V}, V_{DS} = 25\text{V},$ $I_D = 26\text{A}$	Q_g	--	42	--	nC
Total Gate Charge	$V_{GS} = 10\text{V}, V_{DS} = 25\text{V},$ $I_D = 26\text{A}$	Q_g	--	59	--	
Gate-Source Charge		Q_{gs}	--	19	--	
Gate-Drain Charge		Q_{gd}	--	11	--	
Input Capacitance	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V},$ $f = 1.0\text{MHz}$	C_{iss}	--	3794	--	pF
Output Capacitance		C_{oss}	--	785	--	
Reverse Transfer Capacitance		C_{rss}	--	31	--	
Gate Resistance	$f = 1.0\text{MHz}$	R_g	--	0.8	--	Ω
Switching (Note 4)						
Turn-On Delay Time	$V_{GS} = 10\text{V}, V_{DS} = 25\text{V},$ $I_D = 26\text{A}, R_G = 0.8\Omega$	$t_{d(on)}$	--	15.1	--	ns
Rise Time		t_r	--	70.6	--	
Turn-Off Delay Time		$t_{d(off)}$	--	27	--	
Fall Time		t_f	--	5.8	--	
Source-Drain Diode						
Diode Forward Voltage (Note 3)	$V_{GS} = 0\text{V}, I_S = 50\text{A}$	V_{SD}	--	--	1.1	V
Reverse Recovery Time	$I_S = 26\text{A},$ $di/dt = 100\text{A}/\mu\text{s}$	t_{rr}	--	45.3	--	ns
Reverse Recovery Charge		Q_{rr}	--	55.7	--	nC

Notes:

- Package current limit.
- $L = 0.3\text{mH}, V_{GS} = 10\text{V}, R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$.
- Pulse test: Pulse Width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
- Switching time is essentially independent of operating temperature.

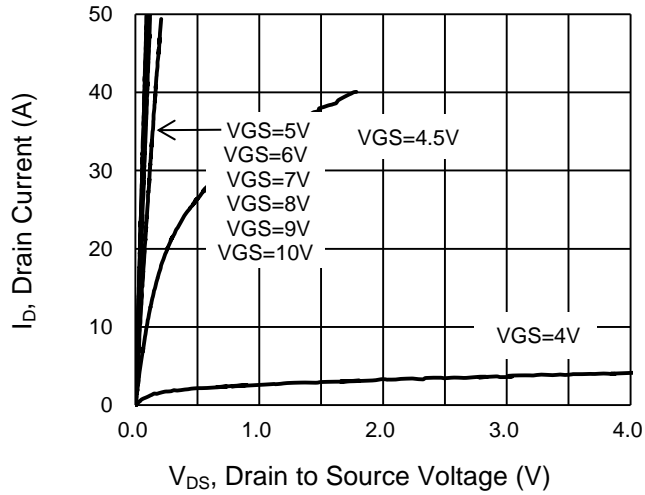
ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TSM025NH04CR RLG	PDFN56U	2,500pcs / 13" Reel

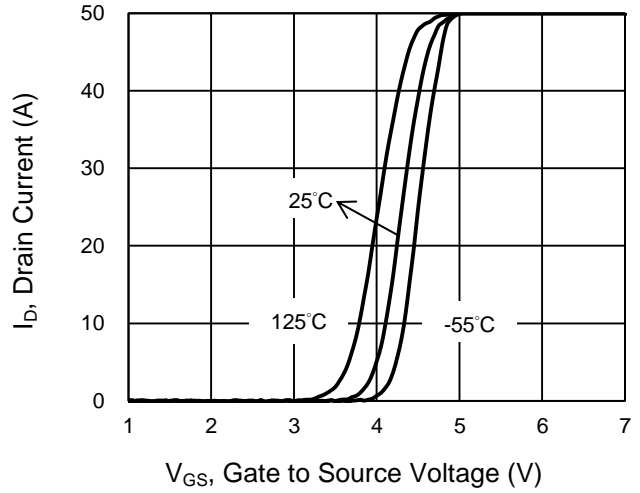
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

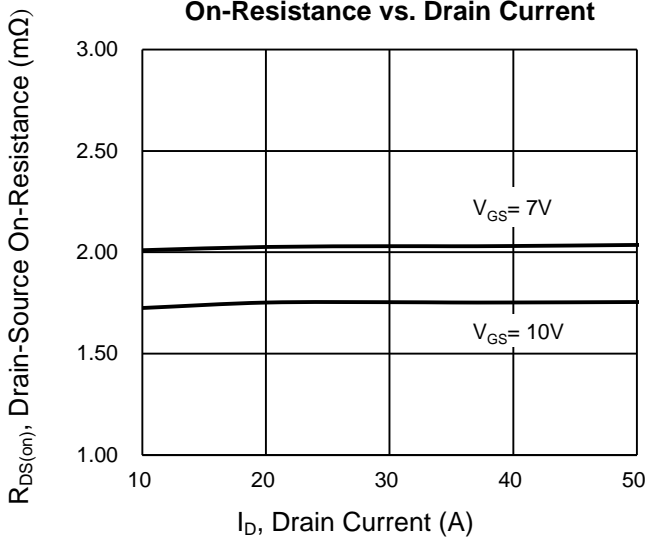
Output Characteristics



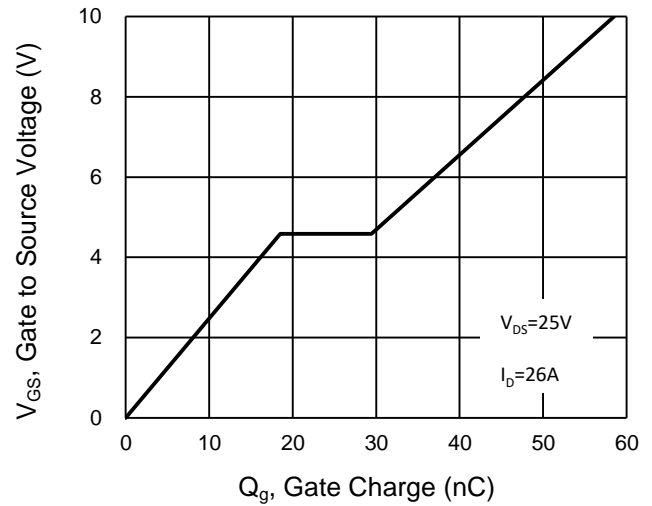
Transfer Characteristics



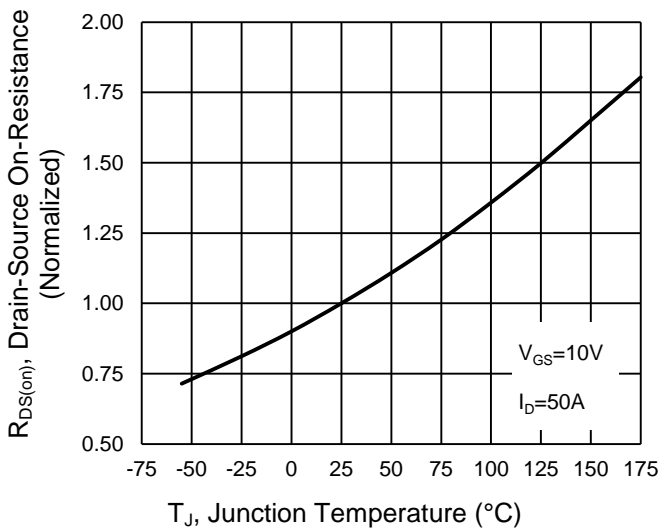
On-Resistance vs. Drain Current



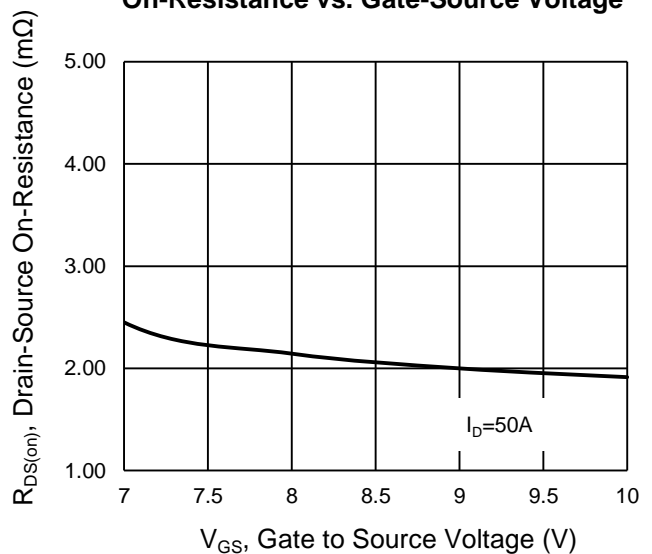
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature

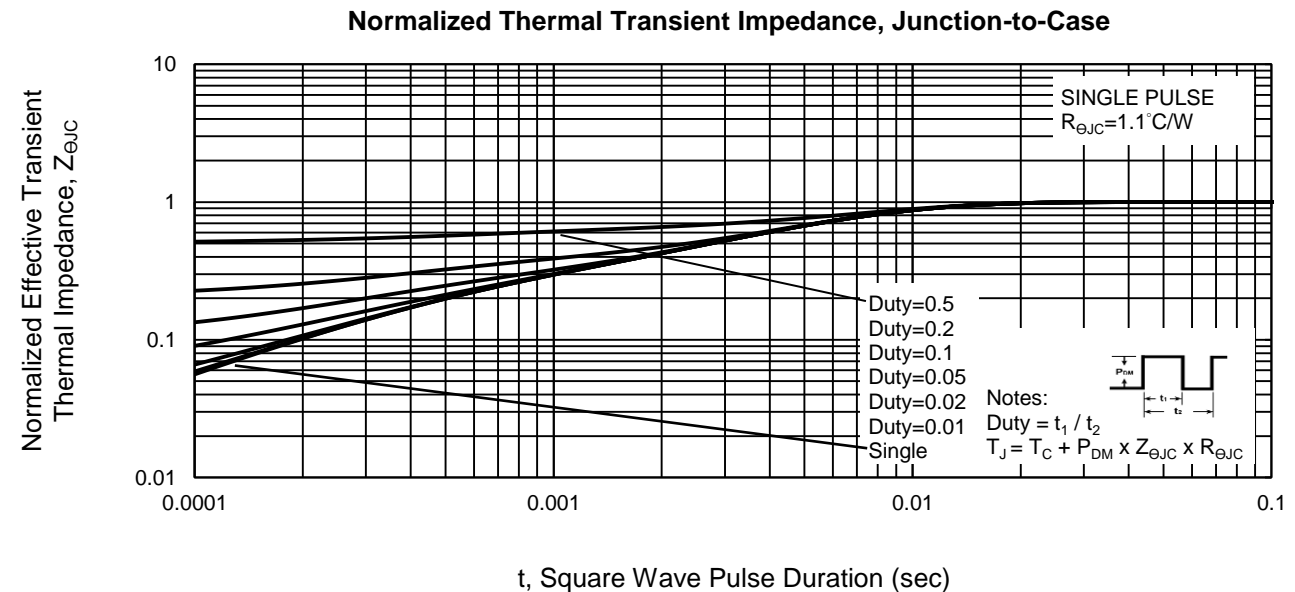
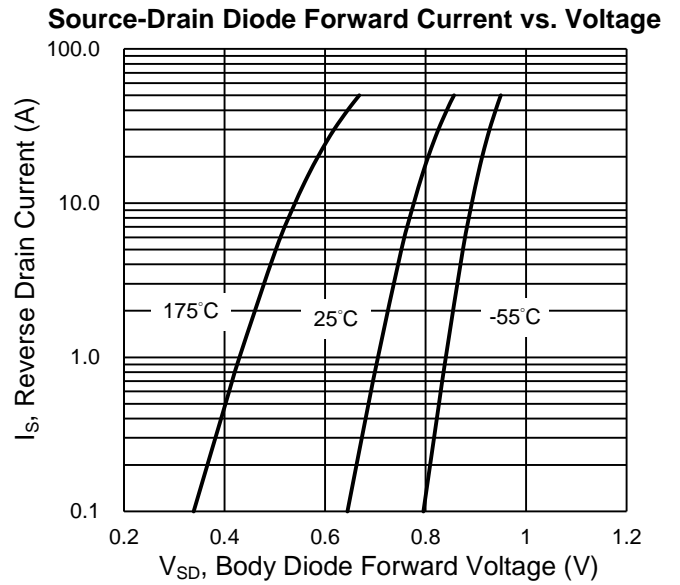
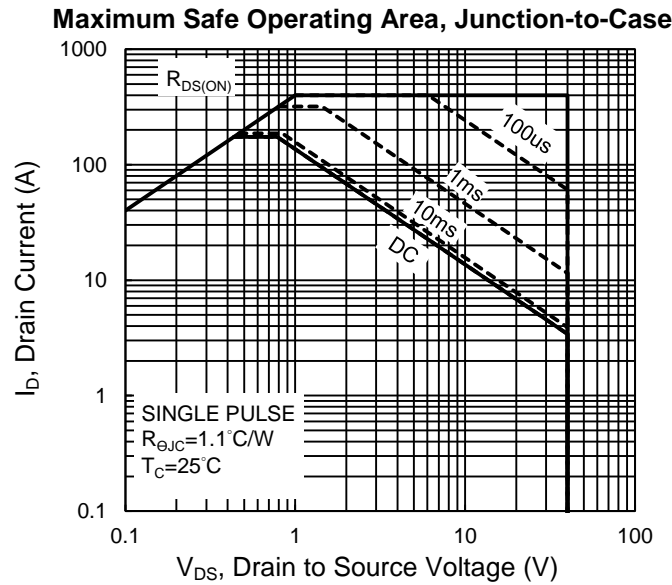
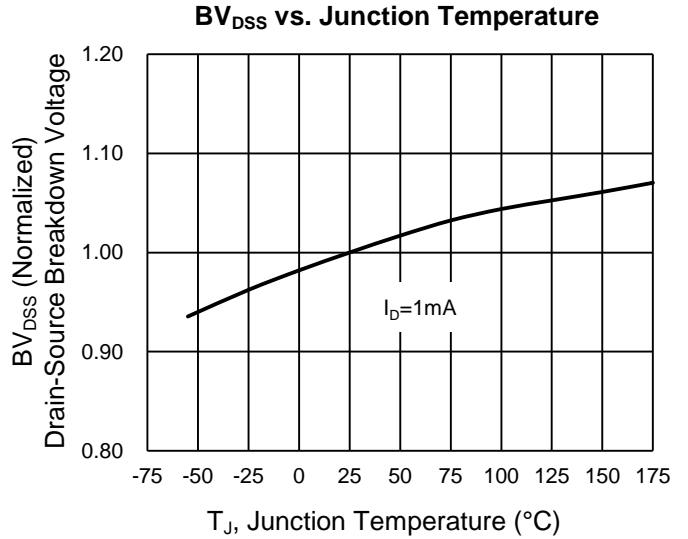
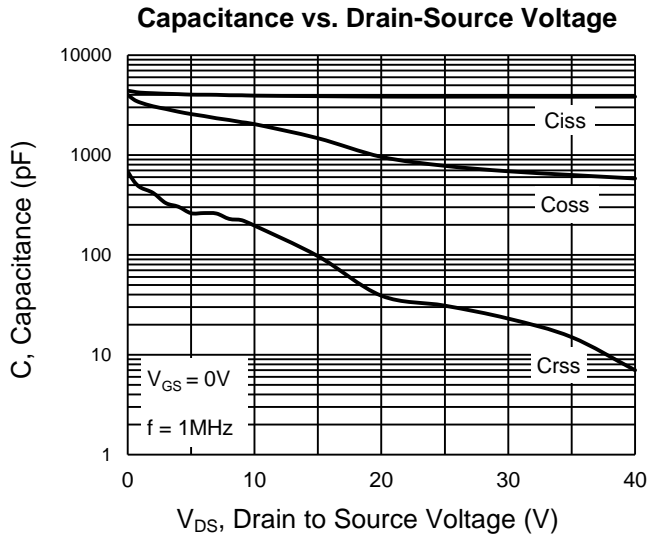


On-Resistance vs. Gate-Source Voltage



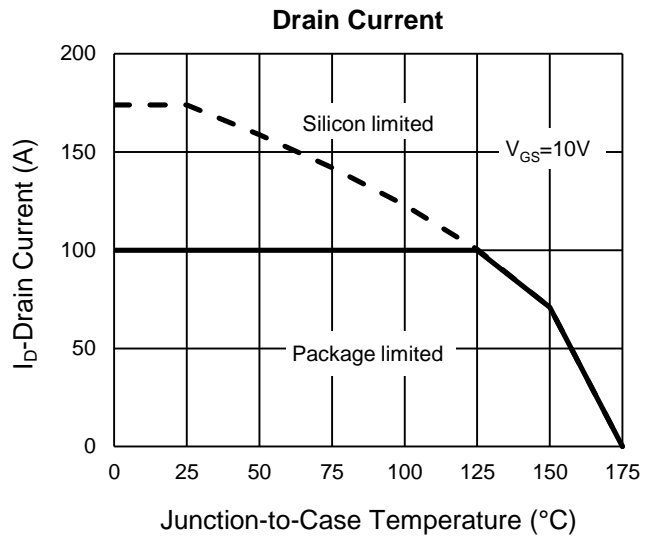
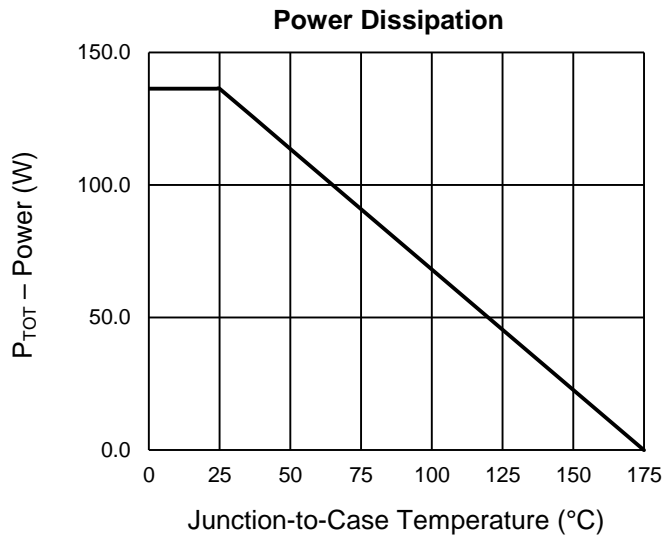
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

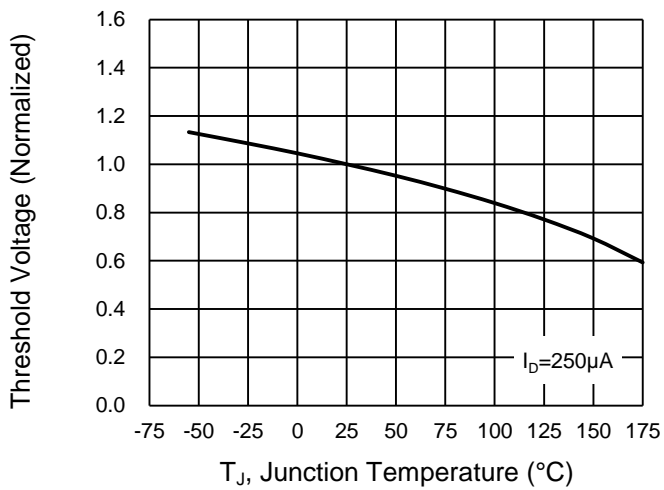


CHARACTERISTICS CURVES

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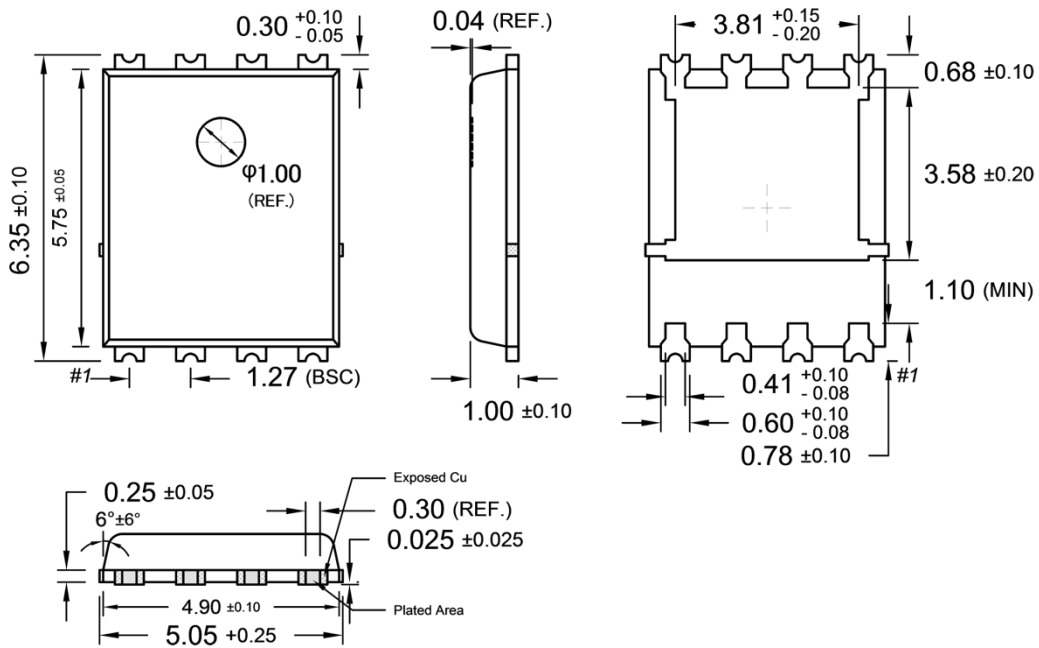


Normalized gate threshold voltage vs Temperature

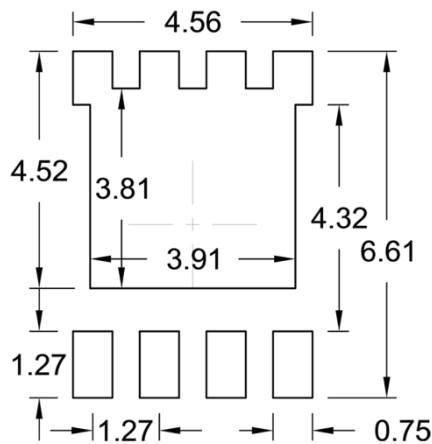


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

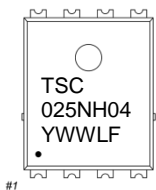
PDFN56U



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



- Y** = Year Code
- WW** = Week Code (01~52)
- L** = Lot Code (1~9,A~Z)
- F** = Factory Code

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