

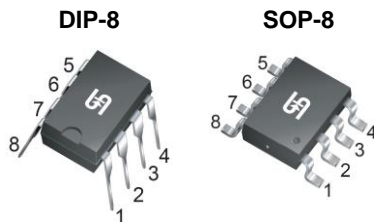
Low Power Low Offset Voltage Dual Comparators

GENERAL DESCRIPTION

The TS393 is dual independent precision voltage comparators capable of single-supply or split-supply operation. The specifications as low as 2.0 mV make this device an excellent ground level with single-supply operation. Input offset-voltage selection for many applications in consumer automotive, and It is designed to permit a common mode range-to- industrial electronics.

FEATURES

- Output voltage compatible with DTL, ECL, TTL, MOS and CMOS Logic levels
- Low input bias current 25nA
- Low input offset current $\pm 0.5nA$
- Low input offset voltage $\pm 2mV$ (typ)
- Input common mode range to ground level
- Differential input voltage range equal to power supply voltage
- Very low supply current drain (0.4mA) – independent of supply voltage
- Wide single-supply range 2V~36V Split-supply range $\pm 1V$ to $\pm 18V$
- RoHS compliant
- Halogen-free

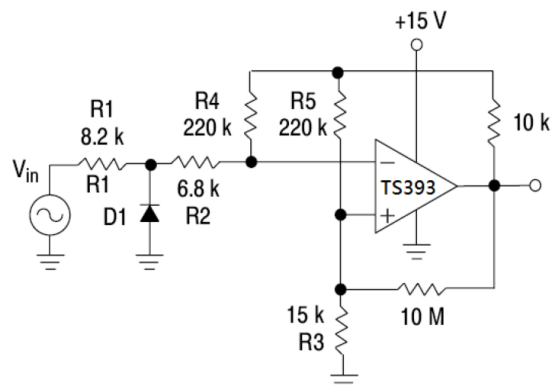


Pin Definition:

- | | |
|----------------|----------------|
| 1. Output A | 5. Input B (+) |
| 2. Input A (-) | 6. Input B (-) |
| 3. Input A (+) | 7. Output B |
| 4. GND | 8. Vcc |

Notes: Moisture sensitivity level: level 3. Per J-STD-020

TYPICAL APPLICATIN CIRCUIT



D1 prevents input from going negative by more than 0.6 V.

$$R1 + R2 = R3$$

$$R3 \leq \frac{R5}{10} \text{ for small error in zero crossing.}$$

Zero Crossing Detector (Single Supply)

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted) (Note 1)			
PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	+36 or ± 18	V
Differential Input Voltage	V_{IDR}	36	V
Input Common Mode Voltage Range	V_{ICR}	-0.3 to 36	V
Input Current	I_{IN}	50	mA
Output Short Circuit to Ground	I_{SC}	Continuous	
Output Sink Current	I_{SINK}	20	mA
Operating Temperature Range	T_{OPR}	0 ~ +70	$^\circ\text{C}$
Junction Temperature	T_J	150	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-65 ~ +150	$^\circ\text{C}$
Lead Temperature 1.6mm (1/16") from case for 10s.	T_{LEAD}	260	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$ unless otherwise noted)					
PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Input Offset Voltage (note 3)	V_{IO}	--	2	5	mV
Input Offset Current $I_{IN(+)} - I_{IN(-)}$, $V_{CM}=0\text{V}$	I_{IO}	--	--	50	nA
Input Offset Current (note 4) $I_{IN(+)} - I_{IN(-)}$, $V_{CM}=0\text{V}$	I_{IB}	--	--	250	nA
Input Common Mode Voltage Range (note 5) $V_{CC}=30\text{V}$	V_{ICR}	-0	--	$V_{CC}-1.5$	V
Voltage Gain $R_L \geq 15\text{K}$, $V_{CC} = 15\text{V}$, $V_o = 1\text{V} \sim 11\text{V}$	A_{VOL}	50	200	--	V/mV
Large Signal Response Time $V_{in} = \text{TTL Logic Swing}$. $V_{REF} = 1.4\text{V}$, $V_{RL} = 5\text{V}$. $R_L = 5.1\text{k}\Omega$	--	--	300	--	ns
Response Time (note 6) $V_{RL} = 5\text{V}$. $R_L = 5.1\text{k}\Omega$	t_{LH}	--	1.3	--	μs
Output Sink Current $V_{IN(-)} = 1\text{V}$, $V_{IN(+)} = 0\text{V}$, $V_o \leq 1.5\text{V}$	I_{SINK}	6.0	16	--	mA
Output Saturation Voltage $V_{IN(-)} = 1\text{V}$, $V_{IN(+)} = 0\text{V}$, $I_{SINK} \leq 4\text{mA}$	V_{OL}	--	250	400	mV
Output Leakage Current $V_{IN(-)} = 0\text{V}$, $V_{IN(+)} = 1\text{V}$, $V_o = 5\text{V}$	I_{OL}	--	0.1	--	nA
Supply Current $R_L = \infty$, $V_{CC} = 5\text{V}$ $R_L = \infty$, $V_{CC} = 36\text{V}$	I_{CC}	--	0.4 1.0	1.0 2.5	mA

ELECTRICAL CHARACTERISTICS

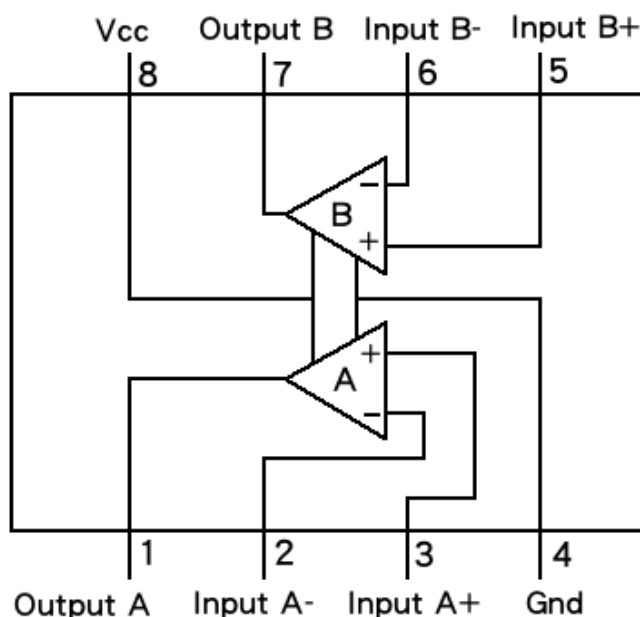
Note:

1. The max. Output current may be as high as 20mA, independent of the magnitude of V_{CC} , output short circuits to V_{CC} can cause excessive heating and eventual destruction.
2. This magnitude of input current will only occur if the input leads are driven more negative than ground or the negative supply voltage. This is due to the input PNP collector base junction becoming forward biased acting as an input clamp diode. There is also a lateral PNP parasitic transistor action on the IC chip. This phenomenon can cause the output voltage of the comparators to go to the V_{CC} voltage level (or ground if overdrive is large) during the time the input is driven negative. This will not destroy the device and normal output states will recover when the inputs become -0.3V of ground or negative supply.
3. At output switch point, $V_O=1.4V_{dc}$, $R_S=0\Omega$ with V_{CC} from 5Vdc to 30Vdc, and over the full input common-mode
4. Due to the PNP transistor inputs, bias current will flow out of the inputs, this current is essentially constant independent of the output state, therefore, no loading changes will exist on the input lines.
5. Input common mode of either input should not be permitted to go more than 0.3V negative of ground or minus supply. The upper limit of common mode range is $V_{CC} - 1.5V$ but either or both inputs can be taken to as high as 30volts without damage.
6. Response time is specified with a 100mV step and 5.0mV of overdrive. With larger magnitudes of overdrive faster response times are obtainable.

ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TS393CD C3G	DIP-8	50pcs / Tube
TS393CS RLG	SOP-8	2,500pcs / 13" Reel

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS CURVE

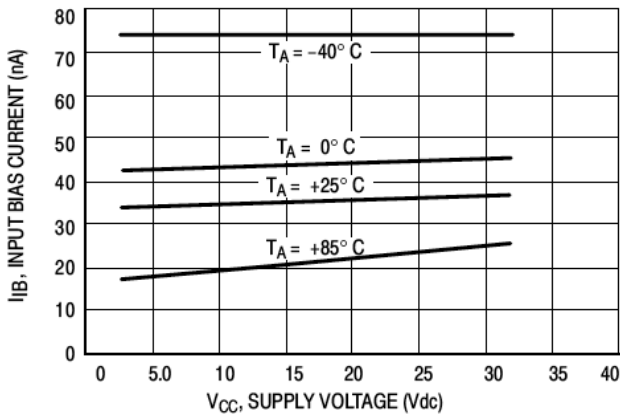


Figure 1. Input Bias Current vs. Power Supply Voltage

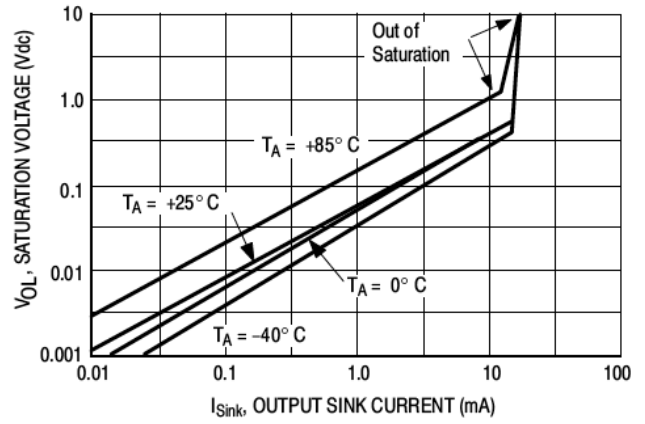


Figure 2. Output Saturation Voltage vs. Output Sink Current

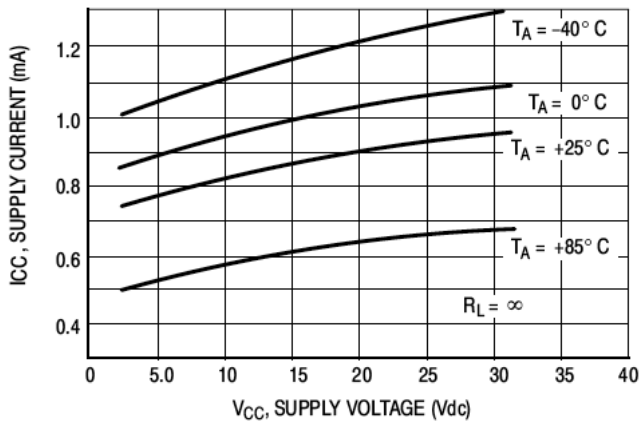


Figure 3. Power Supply Current vs. Power Supply Voltage

APPLICATION INFORMATION

This dual comparator feature high gain, wide bandwidth characteristics. This gives the device oscillation tendencies if the outputs are capacitive coupled to the inputs via stray capacitance. This oscillation manifests itself during output transitions (V_{OL} to V_{OH}). To alleviate this situation input resistors $< 10k\Omega$ should be used. The addition of positive feedback (< 10 mV) is also recommended. It is good design practice to ground all unused pins. Differential input voltages may be larger than supply voltage without damaging the comparator's inputs. Voltages more negative than $-0.3V$ should not be used.

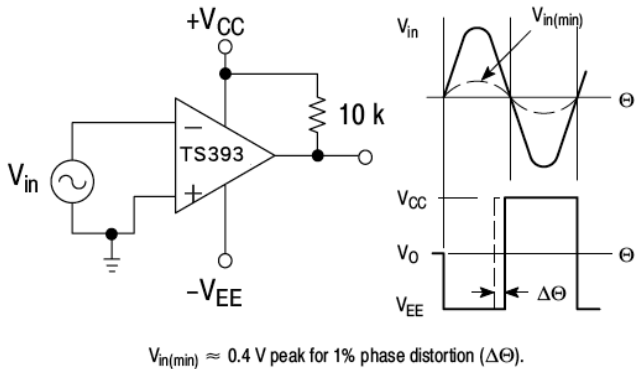


Figure 4. Time Delay Generator

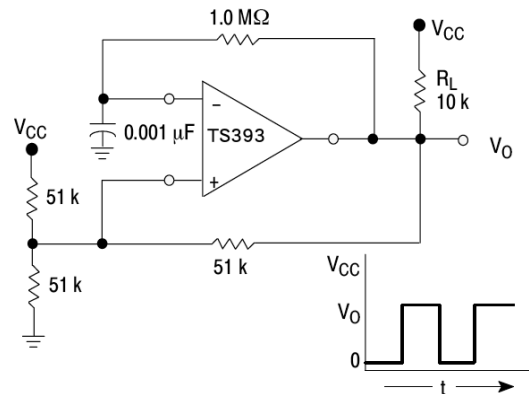


Figure 5. Free-Running Square-Wave Oscillator

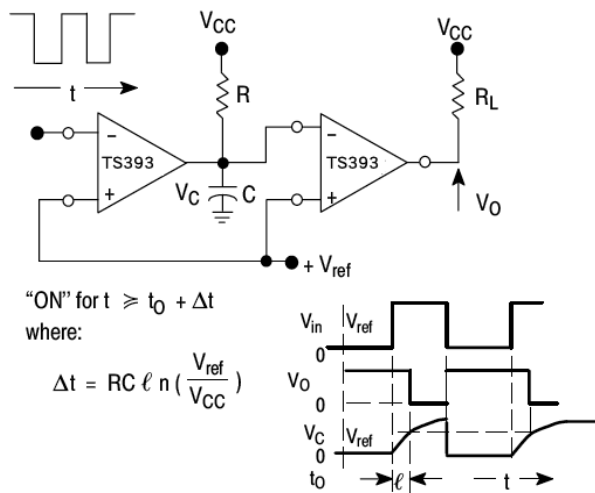


Figure 6. Zero Crossing Detector (Single Supply)

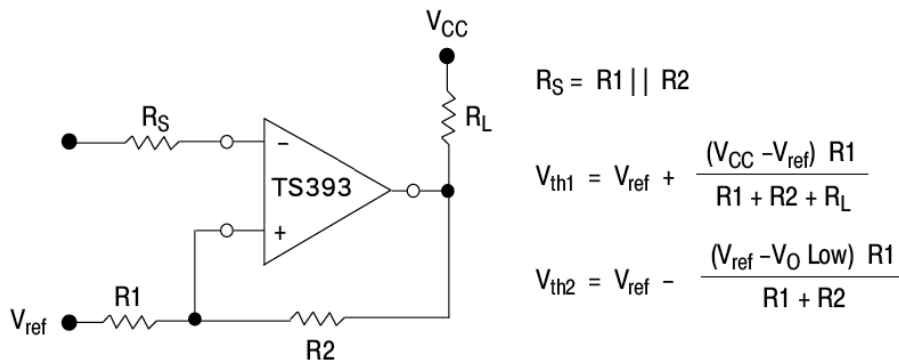
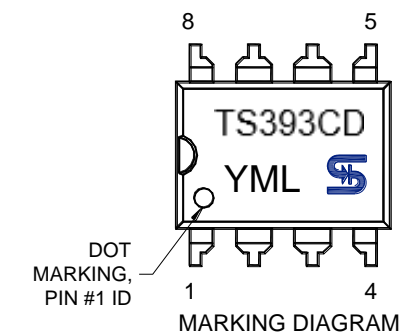
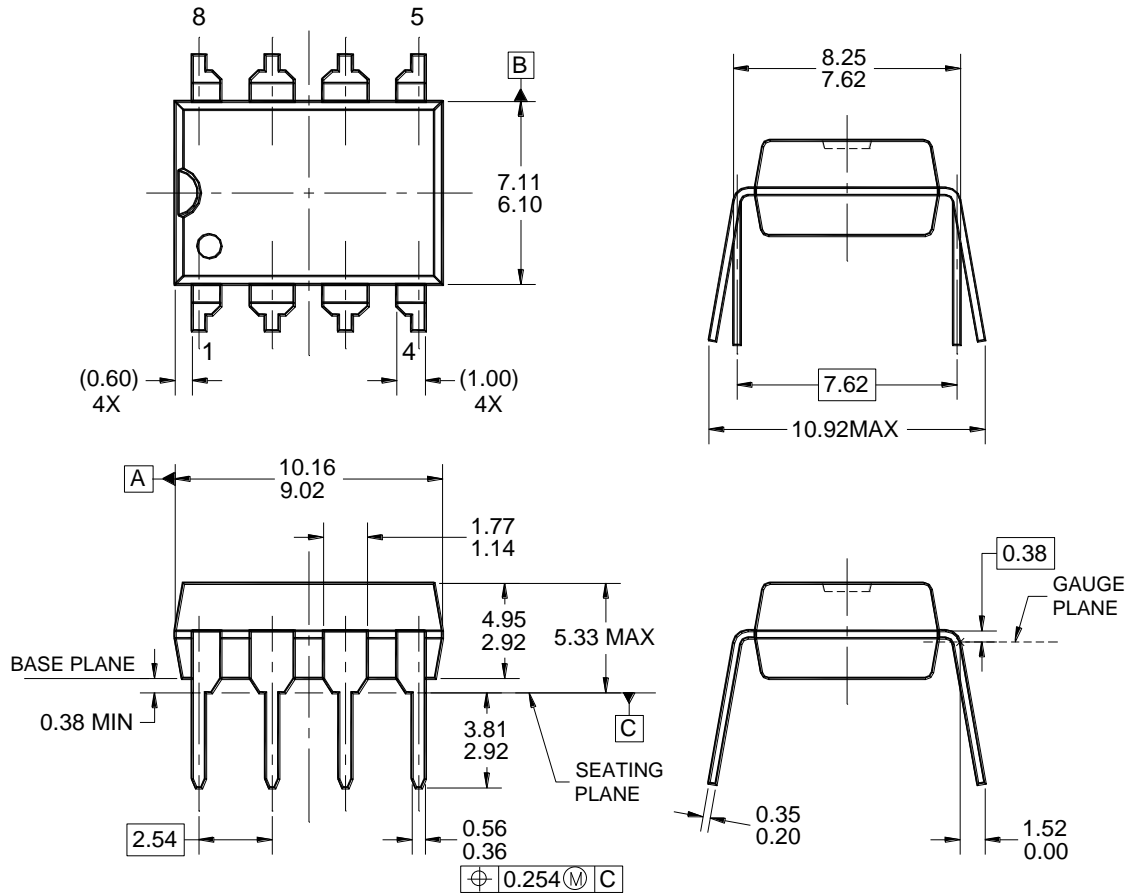


Figure 7. Comparator with Hysteresis

PACKAGE OUTLINE DIMENSIONS

DIP-8



P/N = PRODUCT DEVICE CODE

Y = YEAR CODE

M = MONTH CODE FOR HALOGEN FREE PRODUCT

O = JAN	P = FEB	Q = MAR	R = APR
S = MAY	T = JUN	U = JUL	V = AUG
W = SEP	X = OCT	Y = NOV	Z = DEC

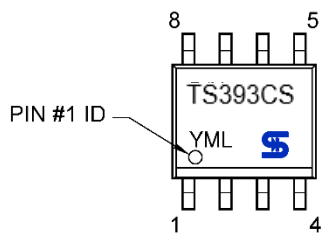
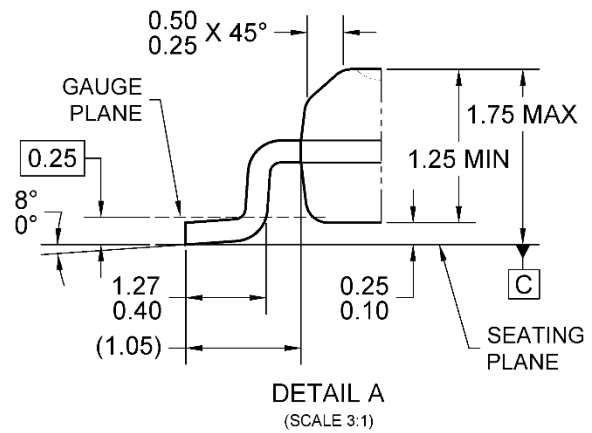
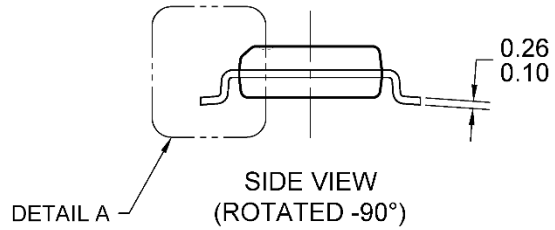
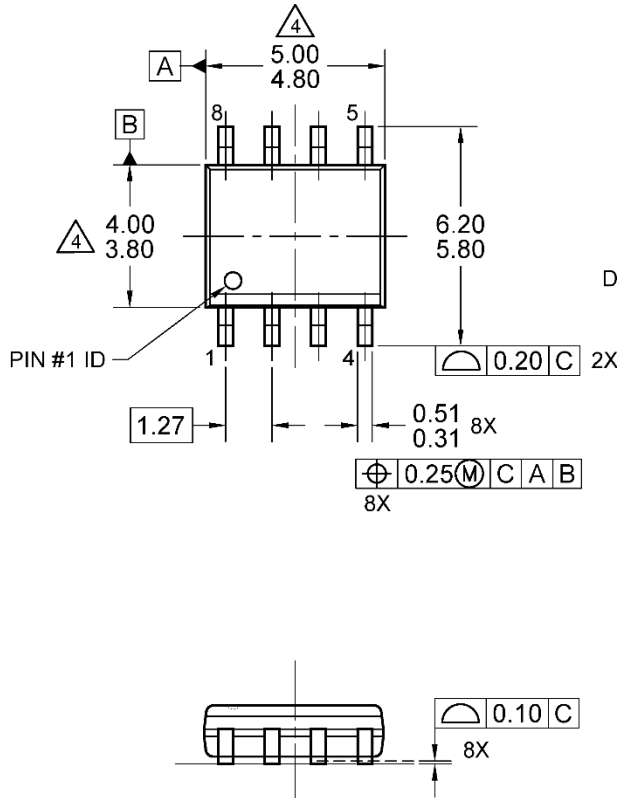
L = LOT CODE

NOTES: UNLESS OTHERWISE SPECIFIED

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2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. THIS CONFORM TO JEDEC PACKAGE REGISTRATION MS-001, VARIATION BA, ISSUE D.
4. DWG NO. REF: HQ2SD07-DIP8-014 REV A.

PACKAGE OUTLINE DIMENSIONS

SOP-8



MARKING DIAGRAM

P/N = PRODUCT DEVICE CODE

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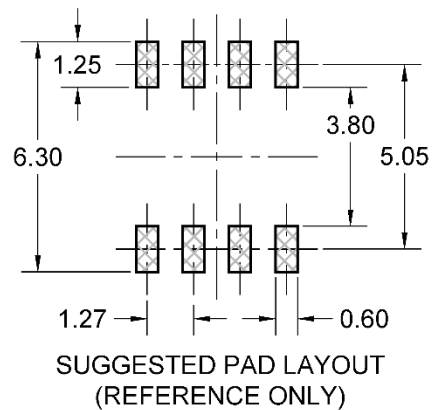
M = MONTH CODE FOR HALOGEN FREE PRODUCT

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2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
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4. MOLDED PLASTIC BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
5. DWG NO REF: HQ2SD07-SOP8STD-028 REV A.

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