

# PerFET™ Power Transistor

## FEATURES

- Excellent FOM
- AEC-Q101 qualified
- Wettable flank leads for enhanced AOI
- 100% UIS and Rg tested
- 175°C operating junction temperature
- RoHS Compliant
- Halogen-free

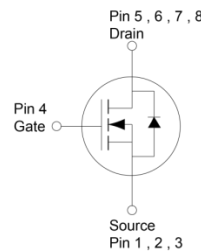
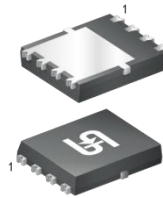
## APPLICATIONS

- Automotive applications
- Solenoid and motor drivers
- DC-DC converters

KEY PERFORMANCE PARAMETERS			
PARAMETER		VALUE	UNIT
$V_{DS}$		100	V
$R_{DS(on)}$ (max)	$V_{GS} = 10V$	17	mΩ
	$V_{GS} = 7V$	20.4	
$Q_g$	$V_{GS} = 10V$	11	nC



PDFN56U



Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$I_D$	$T_C = 25^\circ\text{C}$	50
		$T_C = 100^\circ\text{C}$	36
		$T_A = 25^\circ\text{C}$	9
Pulsed Drain Current (Note 1)	$I_{DM}$	200	A
Single Pulse Avalanche Current (Note 2)	$I_{AS}$	11.3	A
Single Pulse Avalanche Energy (Note 2)	$E_{AS}$	19	mJ
Total Power Dissipation	$P_D$	$T_C = 25^\circ\text{C}$	97
		$T_C = 125^\circ\text{C}$	32
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	- 55 to +175	$^\circ\text{C}$

THERMAL PERFORMANCE			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	1.54	$^\circ\text{C/W}$
Junction to Ambient Thermal Resistance (Note 3)	$R_{\theta JA}$	50	$^\circ\text{C/W}$

### Notes:

1. Pulse Width  $\leq 100\mu\text{s}$ .
2.  $L = 0.3\text{mH}$ ,  $V_{GS} = 10V$ ,  $R_G = 25\Omega$ , Starting  $T_J = 25^\circ\text{C}$ .
3. Device on a PCB FR4 with 1 in<sup>2</sup> (single layer, 2 oz thickness) copper area for drain connection.

**ELECTRICAL SPECIFICATIONS** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 1mA$	$BV_{DSS}$	100	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	$V_{GS(TH)}$	2.4	3	3.6	V
Gate Body Leakage	$V_{GS} = \pm 20V, V_{DS} = 0V$	$I_{GSS}$	--	--	$\pm 100$	nA
Drain-Source Leakage Current	$V_{GS} = 0V, V_{DS} = 100V$	$I_{DSS}$	--	--	1	$\mu A$
	$V_{GS} = 0V, V_{DS} = 100V$ $T_J = 125^\circ\text{C}$		--	--	100	
Drain-Source On-State Resistance (Note 4)	$V_{GS} = 10V, I_D = 25A$	$R_{DS(on)}$	--	13	17	m $\Omega$
	$V_{GS} = 7V, I_D = 25A$		--	16	20.4	
Forward Transconductance (Note 4)	$V_{DS} = 10V, I_D = 6.3A$	$g_{fs}$	--	26	--	S
<b>Dynamic</b> (Note 5)						
Total Gate Charge	$V_{DS} = 50V, I_D = 9A,$ $V_{GS} = 7V$	$Q_g$	--	8.4	--	nC
Total Gate Charge	$V_{DS} = 50V, I_D = 9A,$ $V_{GS} = 10V$	$Q_g$	--	11	--	nC
Gate-Source Charge		$Q_{gs}$	--	3.6	--	
Gate-Drain Charge		$Q_{gd}$	--	2.5	--	
Input Capacitance	$V_{DS} = 60V, V_{GS} = 0V,$ $f = 1.0MHz$	$C_{iss}$	--	725	--	pF
Output Capacitance		$C_{oss}$	--	148	--	
Reverse Transfer Capacitance		$C_{rss}$	--	20	--	
Gate Resistance	$f = 1.0MHz$	$R_g$	--	1.7	--	$\Omega$
<b>Switching</b> (Note 6)						
Turn-On Delay Time	$V_{DD} = 50V, R_G = 6\Omega,$ $I_D = 9A, V_{GS} = 10V$	$t_{d(on)}$	--	7.9	--	ns
Turn-On Rise Time		$t_r$	--	19	--	
Turn-Off Delay Time		$t_{d(off)}$	--	13	--	
Turn-Off Fall Time		$t_f$	--	21	--	
<b>Source-Drain Diode</b>						
Forward Voltage (Note 4)	$I_S = 25A, V_{GS} = 0V$	$V_{SD}$	--	--	1.1	V
Reverse Recovery Time	$I_S = 9A,$ $di/dt = 100A/\mu s$	$t_{rr}$	--	50	--	ns
Reverse Recovery Charge		$Q_{rr}$	--	64	--	nC

**Notes:**

- Pulse test: Pulse Width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$ .
- Defined by design. Not subject to production test.
- Switching time is essentially independent of operating temperature.

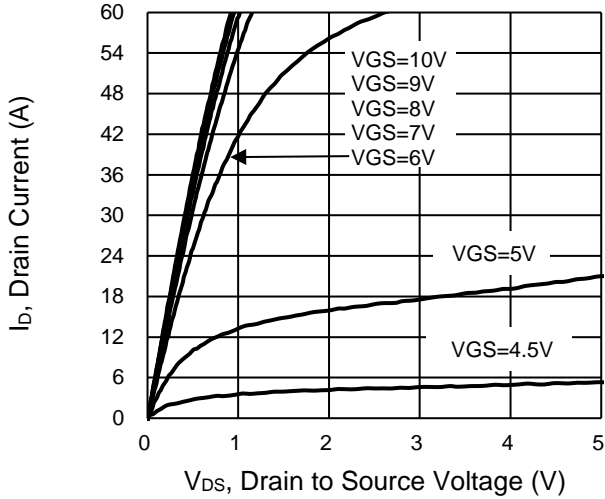
**ORDERING INFORMATION**

ORDERING CODE	PACKAGE	PACKING
TQM170NH10CR RLG	PDFN56U	2,500pcs / 13" Reel

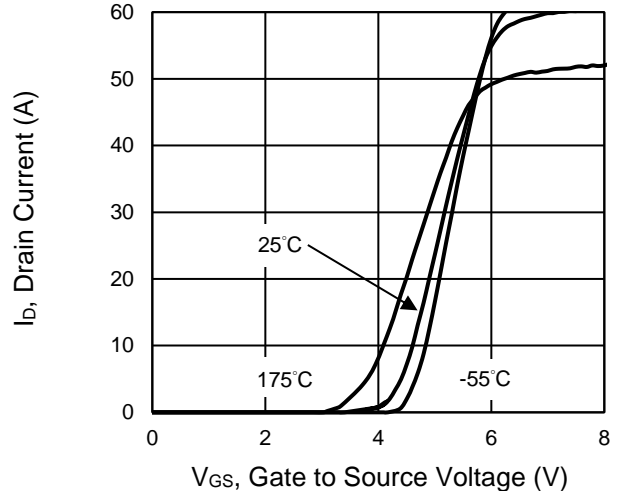
**CHARACTERISTICS CURVES**

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

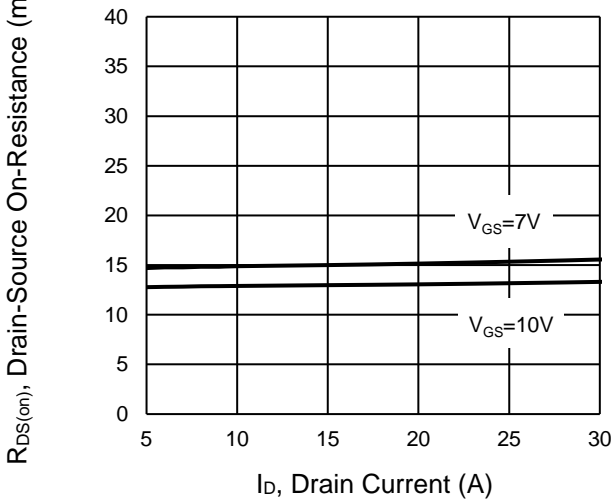
**Output Characteristics**



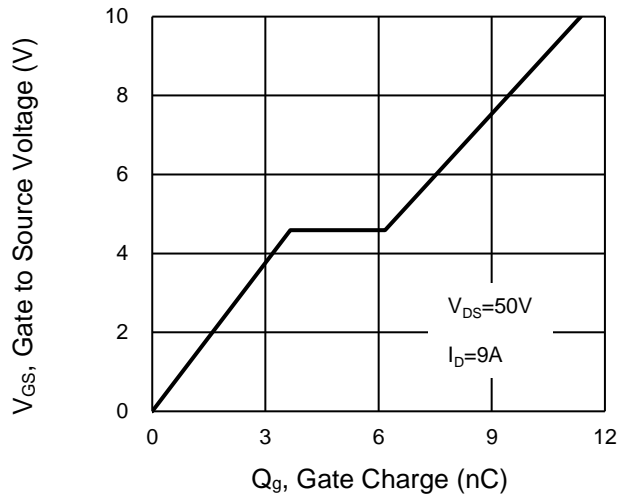
**Transfer Characteristics**



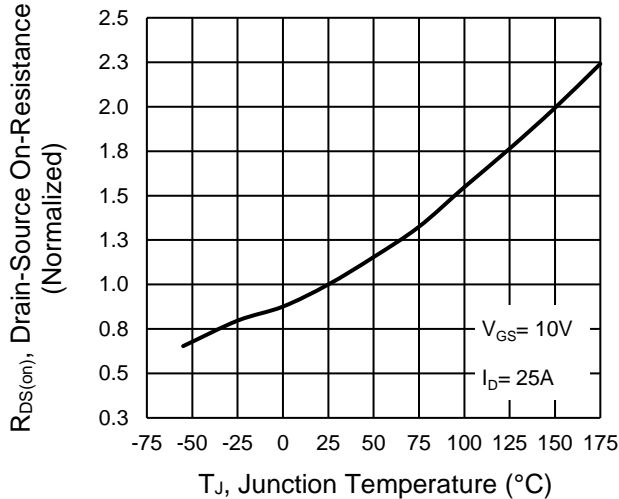
**On-Resistance vs. Drain Current**



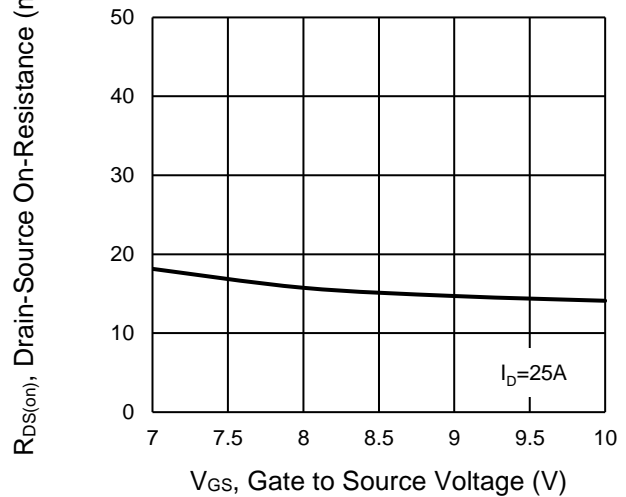
**Gate-Source Voltage vs. Gate Charge**



**On-Resistance vs. Junction Temperature**



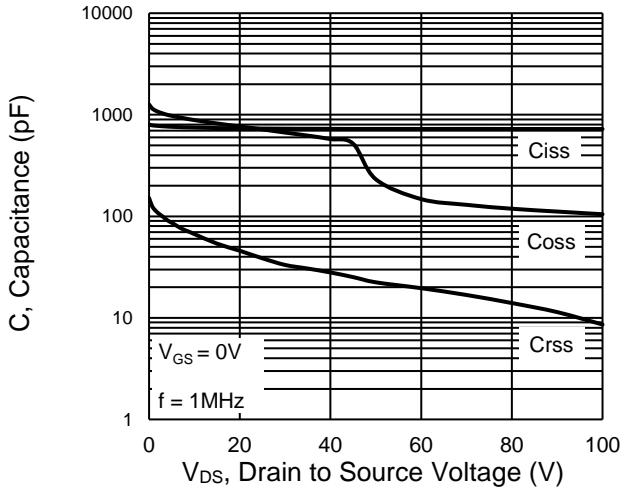
**On-Resistance vs. Gate-Source Voltage**



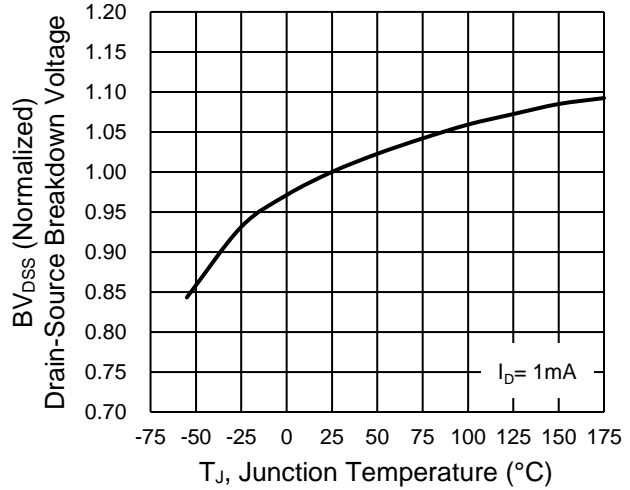
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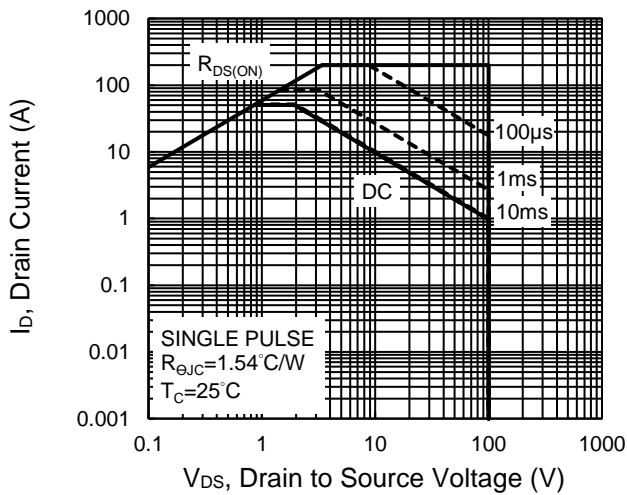
**Capacitance vs. Drain-Source Voltage**



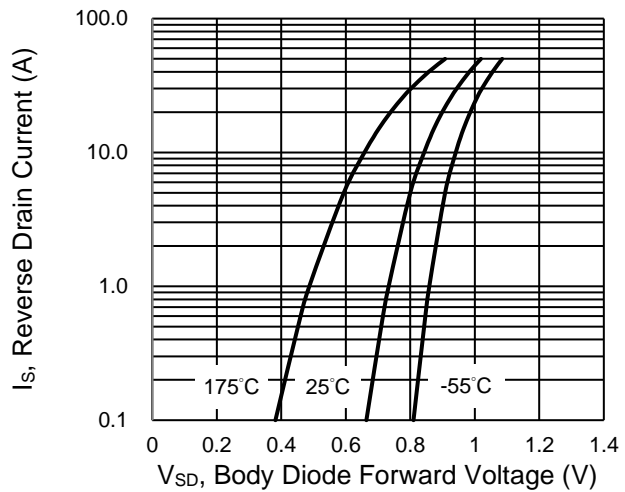
**$BV_{DSS}$  vs. Junction Temperature**



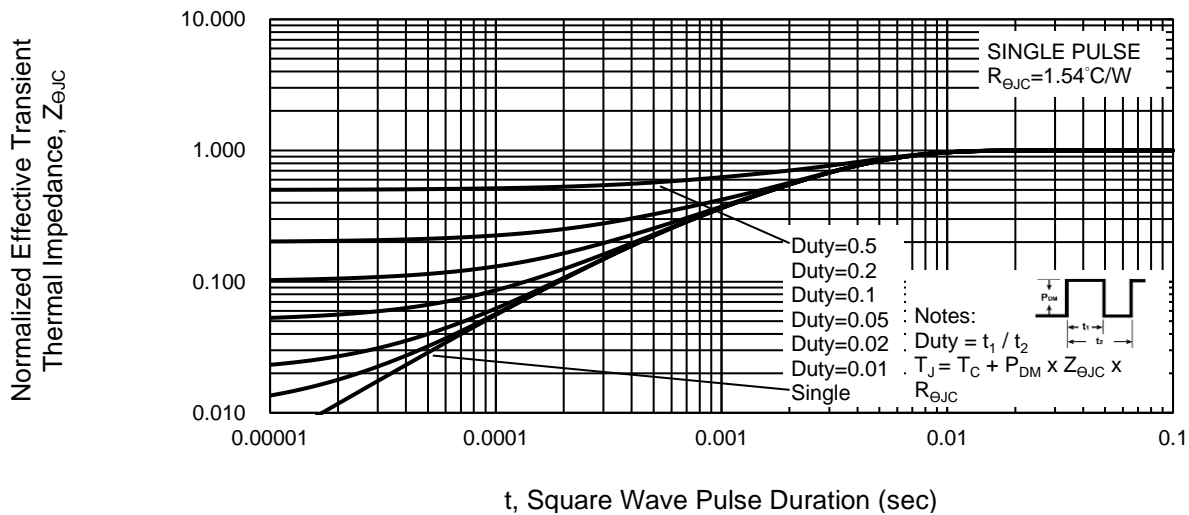
**Maximum Safe Operating Area, Junction-to-Case**



**Source-Drain Diode Forward Current vs. Voltage**



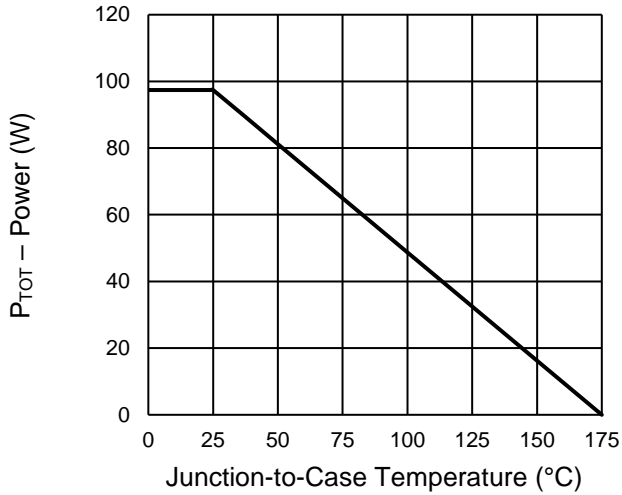
**Normalized Thermal Transient Impedance, Junction-to-Case**



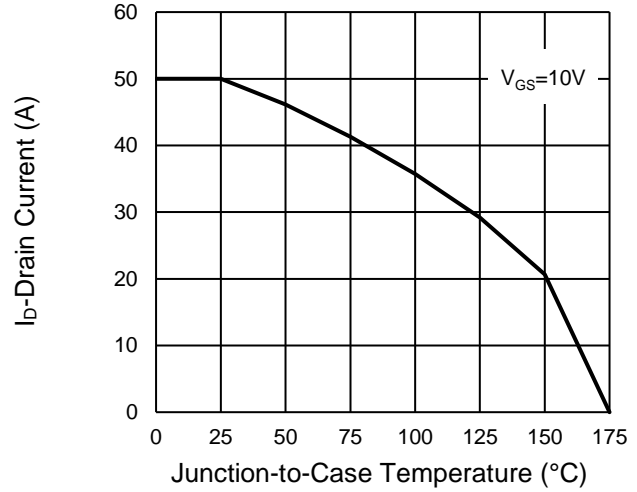
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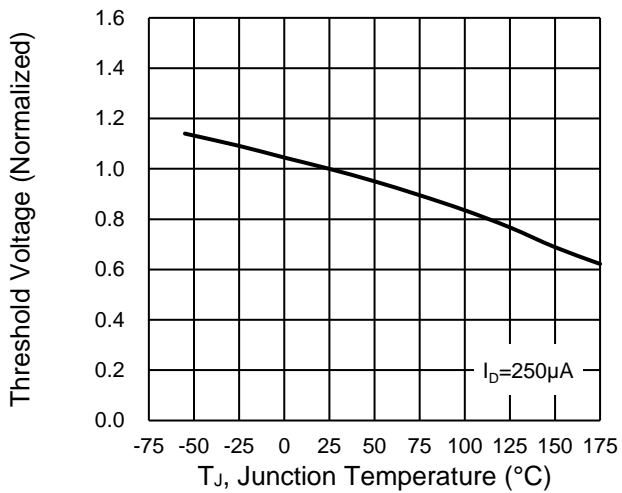
**Power Dissipation**



**Drain Current**

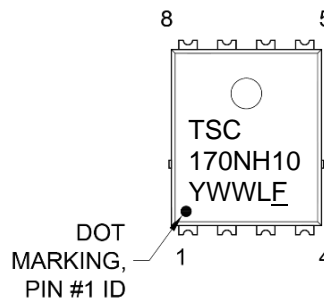
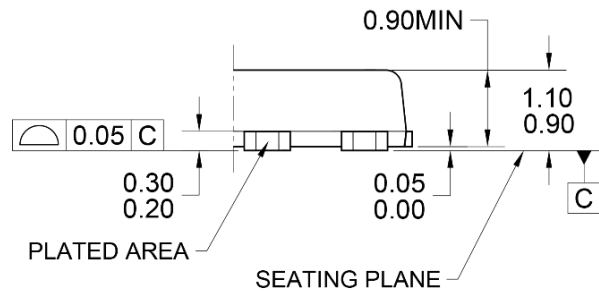
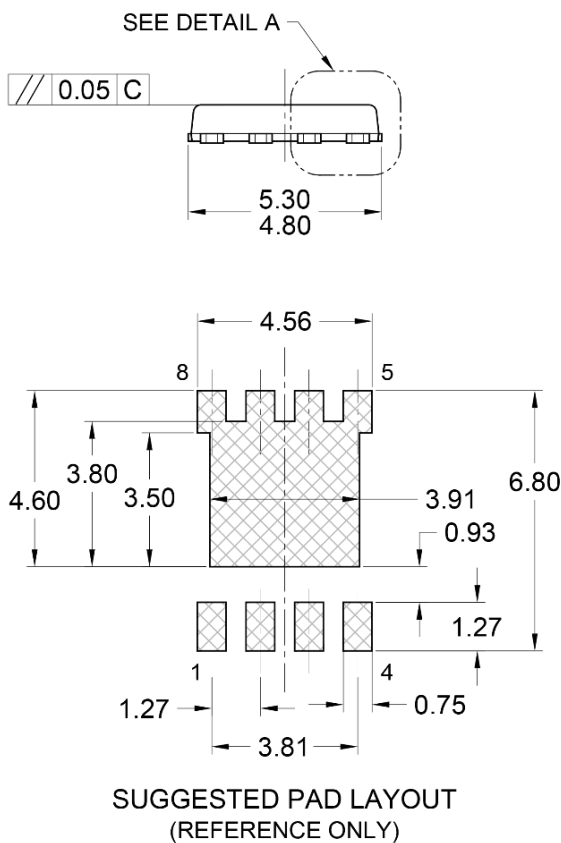
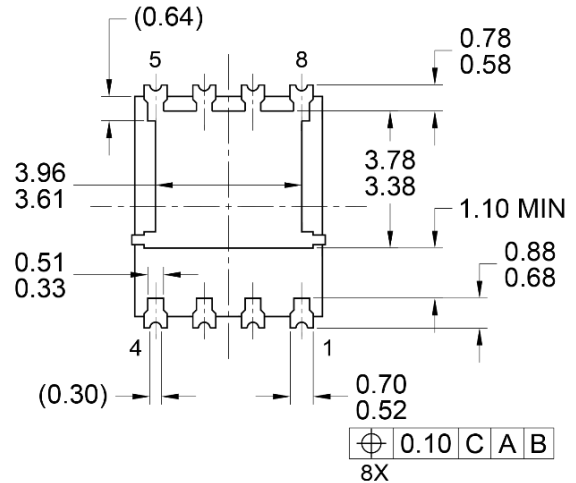
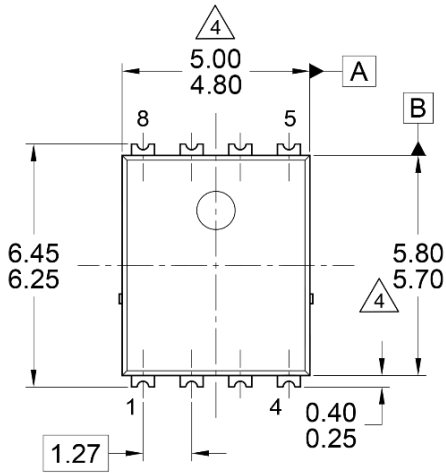


**Normalized gate threshold voltage vs Temperature**



**PACKAGE OUTLINE DIMENSIONS** (Unit: Millimeters)

PDFN56U



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PACKAGE OUTLINE REFERENCE: JEITA ED-7500B, EIAJ SC-111BB.
4. MOLDED PLASTIC BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
5. DWG NO. REF: HQ2SD07-PDFN56U-023 REV B.

MARKING DIAGRAM

- 170NH10 = Device marking  
 Y = Year code  
 WW = Week code (01~52)  
 L = Lot code (1~9,A~Z)  
 F = Factory code  
 - = AEC-Q101 qualified

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