

PerFET™ Power Transistor

FEATURES

- Excellent FOM
- AEC-Q101 qualified
- Wettable flank leads for enhanced AOI
- 100% UIS and Rg tested
- 175°C operating junction temperature
- RoHS Compliant
- Halogen-free

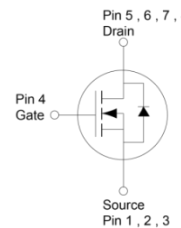
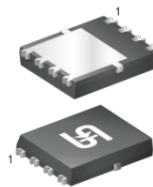
APPLICATIONS

- Automotive applications
- Solenoid and motor drivers
- DC-DC converters

| KEY PERFORMANCE PARAMETERS | | | |
|----------------------------|----------------|-------|------|
| PARAMETER | | VALUE | UNIT |
| V_{DS} | | 80 | V |
| $R_{DS(on)}$ (max) | $V_{GS} = 10V$ | 6.3 | mΩ |
| | $V_{GS} = 7V$ | 7.6 | |
| Q_g | $V_{GS} = 10V$ | 27 | nC |



PDFN56U



Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

| ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted) | | | | |
|-----------------------------------------------------------------------------|---------------------------|----------------|--------------|------------------|
| PARAMETER | | SYMBOL | LIMIT | UNIT |
| Drain-Source Voltage | | V_{DS} | 80 | V |
| Gate-Source Voltage | | V_{GS} | ± 20 | V |
| Continuous Drain Current, Silicon limited | $T_C = 25^\circ\text{C}$ | I_D | 106 | A |
| Continuous Drain Current (Note 1) | $T_C = 25^\circ\text{C}$ | I_D | 100 | A |
| | $T_C = 100^\circ\text{C}$ | | 75 | |
| | $T_A = 25^\circ\text{C}$ | | 15 | |
| Pulsed Drain Current (Note 2) | | I_{DM} | 424 | A |
| Single Pulse Avalanche Current (Note 3) | | I_{AS} | 26.2 | A |
| Single Pulse Avalanche Energy (Note 3) | | E_{AS} | 103 | mJ |
| Total Power Dissipation | $T_C = 25^\circ\text{C}$ | P_D | 153 | W |
| | $T_C = 125^\circ\text{C}$ | | 51 | |
| Operating Junction and Storage Temperature Range | | T_J, T_{STG} | - 55 to +175 | $^\circ\text{C}$ |

| THERMAL PERFORMANCE | | | |
|-------------------------------------------------|-----------------|-------|--------------------|
| PARAMETER | SYMBOL | LIMIT | UNIT |
| Junction to Case Thermal Resistance | $R_{\theta JC}$ | 0.98 | $^\circ\text{C/W}$ |
| Junction to Ambient Thermal Resistance (Note 4) | $R_{\theta JA}$ | 50 | $^\circ\text{C/W}$ |

Notes:

1. Package current limit.
2. Pulse Width $\leq 100\mu\text{s}$.
3. $L = 0.3\text{mH}$, $V_{GS} = 10V$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$.
4. Device on a PCB FR4 with 1 in² (single layer, 2 oz thickness) copper area for drain connection.

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| PARAMETER | CONDITIONS | SYMBOL | MIN | TYP | MAX | UNIT |
|----------------------------------------------|-------------------------------------------------------------|--------------|-----|------|-----------|------------|
| Static | | | | | | |
| Drain-Source Breakdown Voltage | $V_{GS} = 0V, I_D = 1mA$ | BV_{DSS} | 80 | -- | -- | V |
| Gate Threshold Voltage | $V_{DS} = V_{GS}, I_D = 250\mu A$ | $V_{GS(TH)}$ | 2.4 | 3.1 | 3.6 | V |
| Gate Body Leakage | $V_{GS} = \pm 20V, V_{DS} = 0V$ | I_{GSS} | -- | -- | ± 100 | nA |
| Drain-Source Leakage Current | $V_{GS} = 0V, V_{DS} = 80V$ | I_{DSS} | -- | -- | 1 | μA |
| | $V_{GS} = 0V, V_{DS} = 80V$ $T_J = 125^\circ\text{C}$ | | -- | -- | 100 | |
| Drain-Source On-State Resistance (Note 5) | $V_{GS} = 10V, I_D = 50A$ | $R_{DS(on)}$ | -- | 5.3 | 6.3 | m Ω |
| | $V_{GS} = 7V, I_D = 50A$ | | -- | 6.5 | 7.6 | |
| Forward Transconductance (Note 5) | $V_{DS} = 10V, I_D = 12.5A$ | g_{fs} | -- | 49 | -- | S |
| Dynamic (Note 6) | | | | | | |
| Total Gate Charge | $V_{DS} = 40V, I_D = 15A,$ $V_{GS} = 7V$ | Q_g | -- | 20 | -- | nC |
| Total Gate Charge | $V_{DS} = 40V, I_D = 15A,$ $V_{GS} = 10V$ | Q_g | -- | 27 | -- | nC |
| Gate-Source Charge | | Q_{gs} | -- | 9.3 | -- | |
| Gate-Drain Charge | | Q_{gd} | -- | 5.9 | -- | |
| Input Capacitance | $V_{DS} = 40V, V_{GS} = 0V,$ $f = 1.0MHz$ | C_{iss} | -- | 1832 | -- | pF |
| Output Capacitance | | C_{oss} | -- | 1240 | -- | |
| Reverse Transfer Capacitance | | C_{rss} | -- | 54 | -- | |
| Gate Resistance | $f = 1.0MHz$ | R_g | -- | 0.5 | -- | Ω |
| Switching (Note 7) | | | | | | |
| Turn-On Delay Time | $V_{DD} = 40V, R_G = 6\Omega,$ $I_D = 15A, V_{GS} = 10V$ | $t_{d(on)}$ | -- | 14 | -- | ns |
| Turn-On Rise Time | | t_r | -- | 34 | -- | |
| Turn-Off Delay Time | | $t_{d(off)}$ | -- | 22 | -- | |
| Turn-Off Fall Time | | t_f | -- | 29 | -- | |
| Source-Drain Diode | | | | | | |
| Forward Voltage (Note 5) | $I_S = 50A, V_{GS} = 0V$ | V_{SD} | -- | -- | 1.1 | V |
| Reverse Recovery Time | $I_S = 15A,$ $di/dt = 100A/\mu s$ | t_{rr} | -- | 68 | -- | ns |
| Reverse Recovery Charge | | Q_{rr} | -- | 104 | -- | nC |

Notes:

5. Pulse test: Pulse Width $\leq 300\mu s$, duty cycle $\leq 2\%$.
6. Defined by design. Not subject to production test.
7. Switching time is essentially independent of operating temperature.

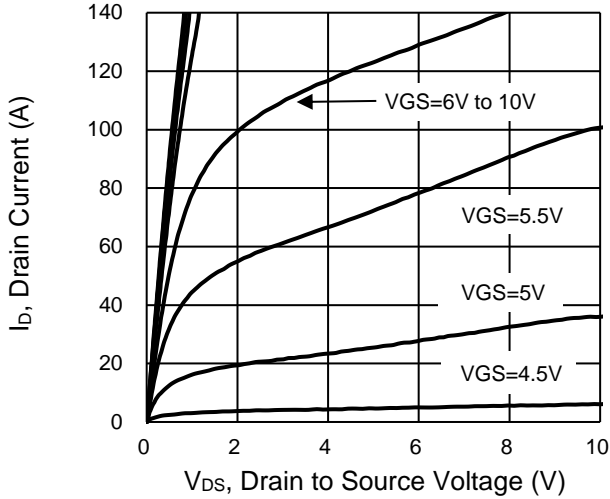
ORDERING INFORMATION

| ORDERING CODE | PACKAGE | PACKING |
|------------------|---------|---------------------|
| TQM063NH08CR RLG | PDFN56U | 2,500pcs / 13" Reel |

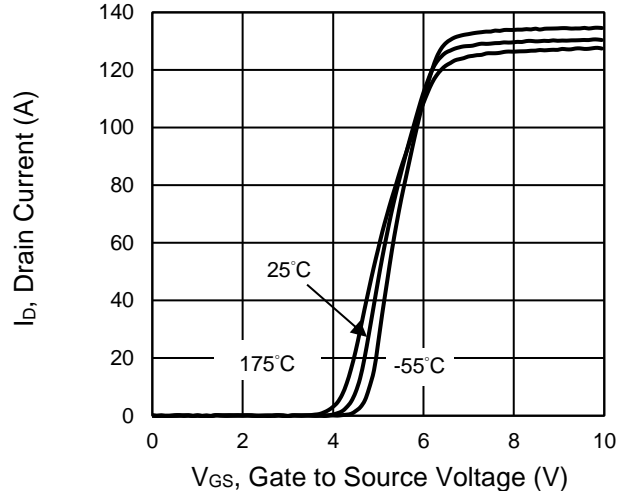
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

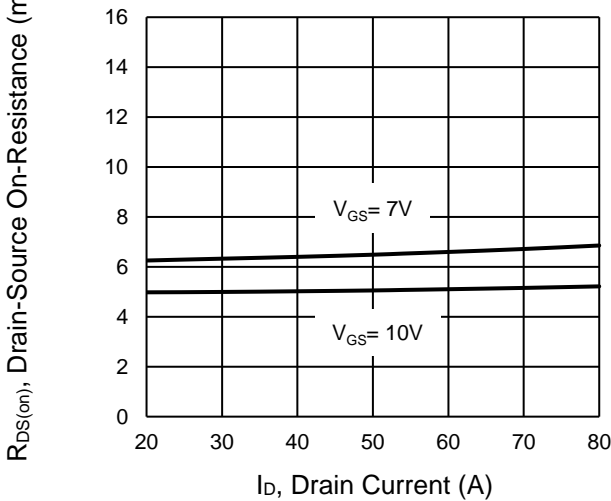
Output Characteristics



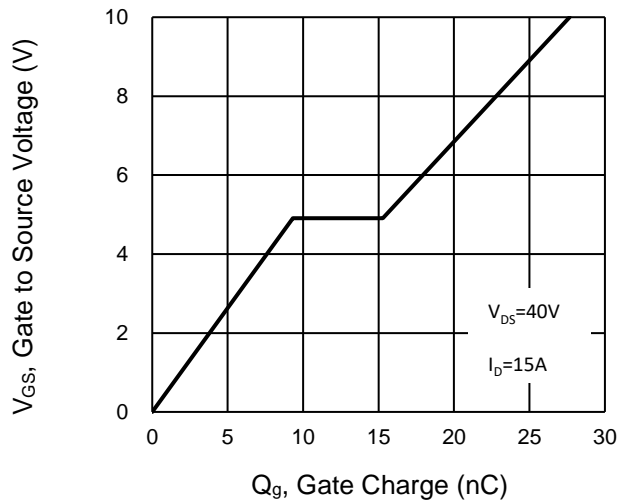
Transfer Characteristics



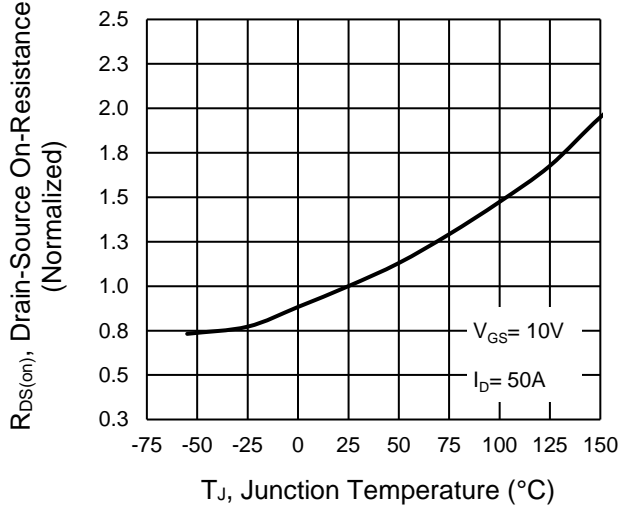
On-Resistance vs. Drain Current



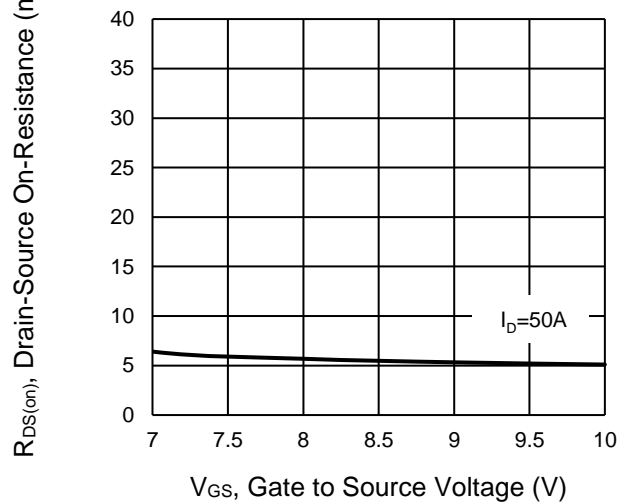
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



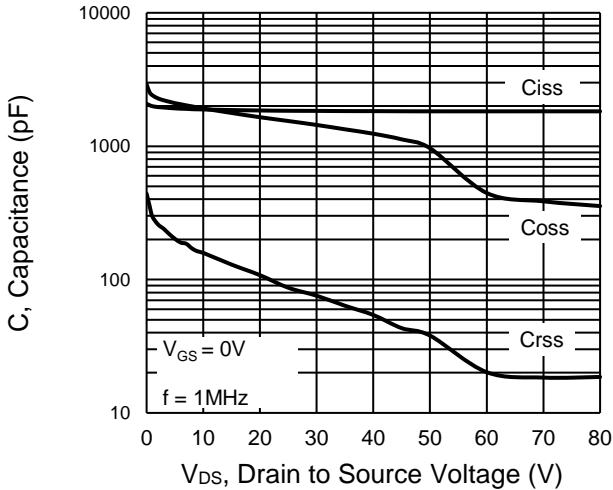
On-Resistance vs. Gate-Source Voltage



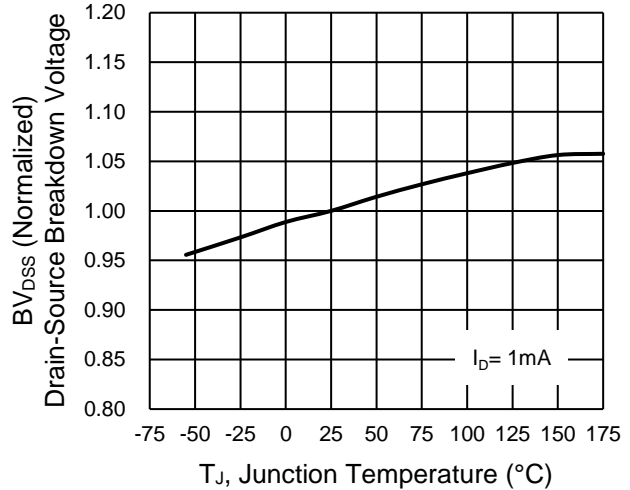
CHARACTERISTICS CURVES

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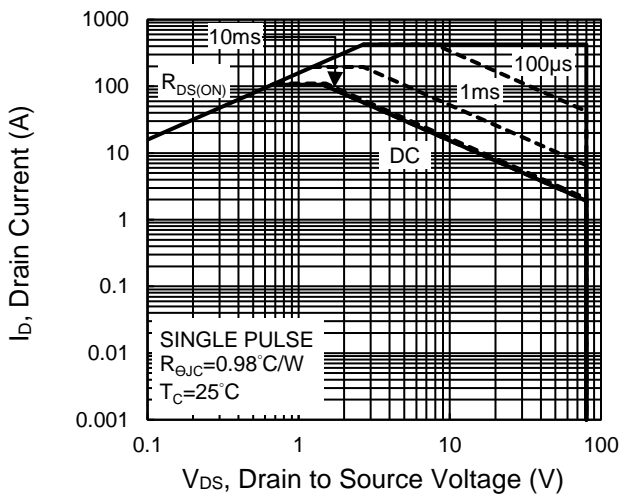
Capacitance vs. Drain-Source Voltage



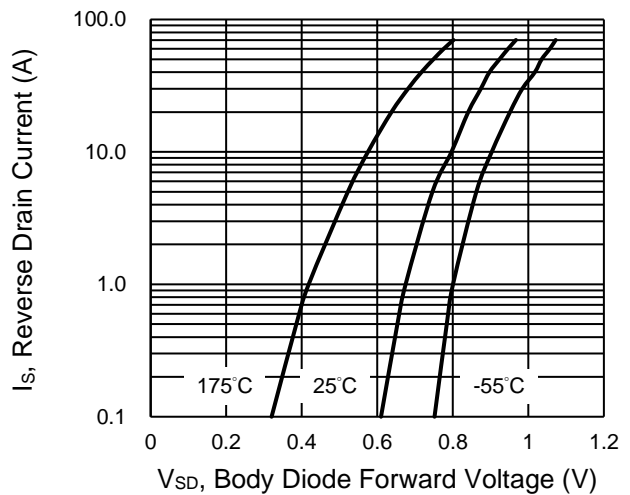
BV_{DSS} vs. Junction Temperature



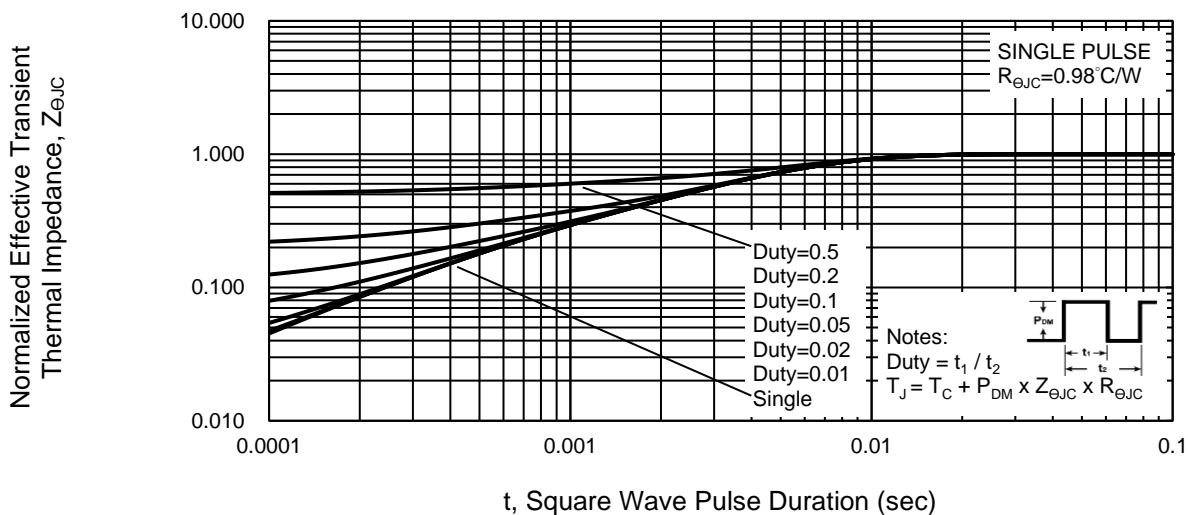
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage



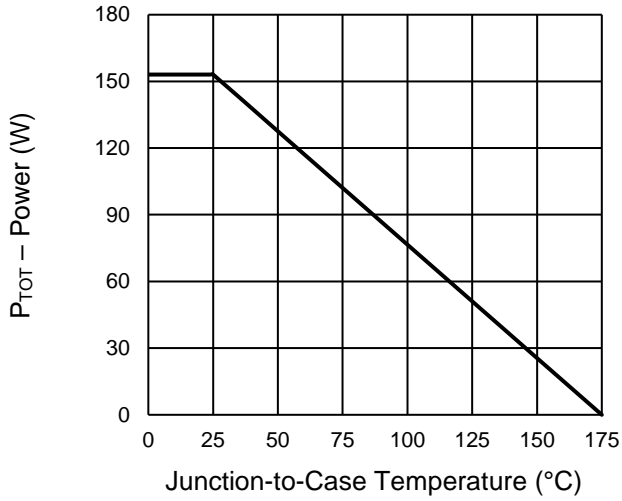
Normalized Thermal Transient Impedance, Junction-to-Case



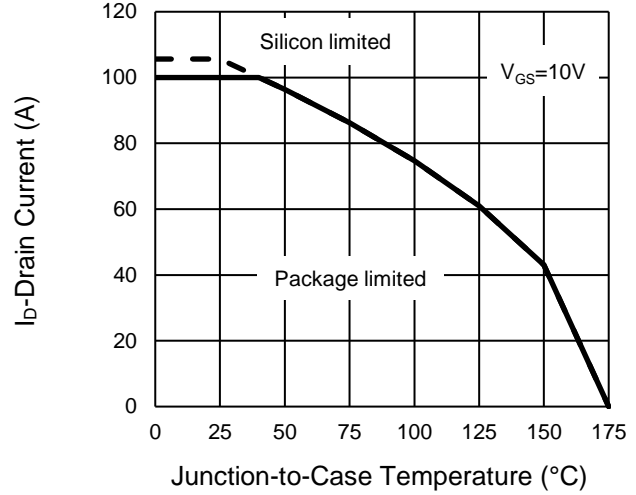
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

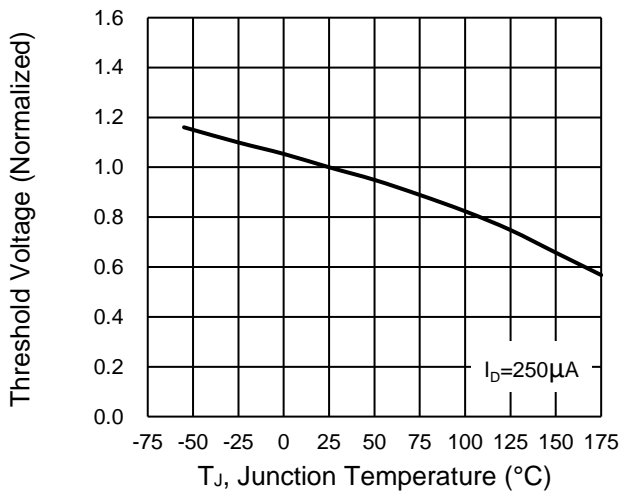
Power Dissipation



Drain Current

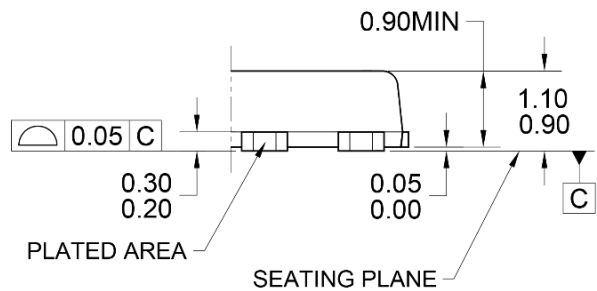
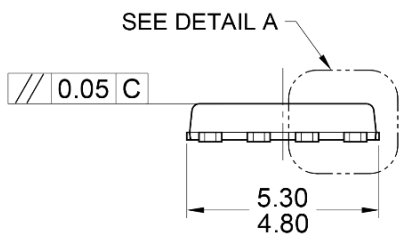
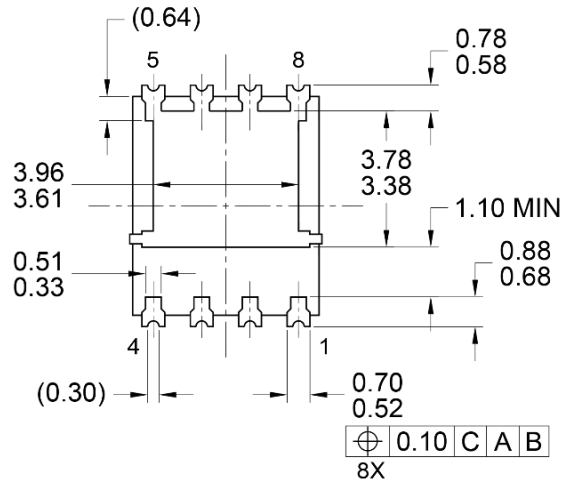
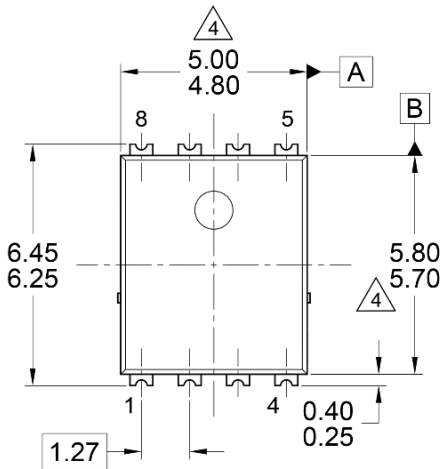


Normalized gate threshold voltage vs Temperature

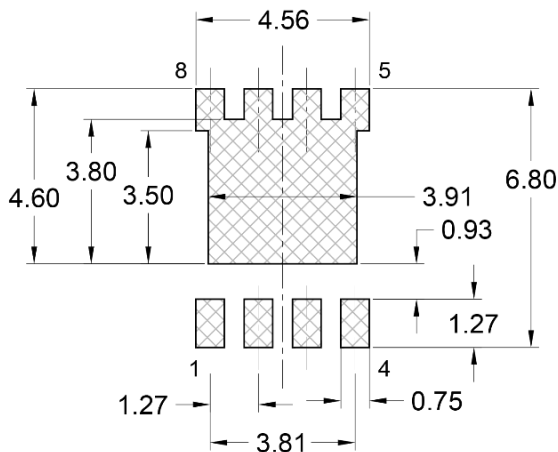


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

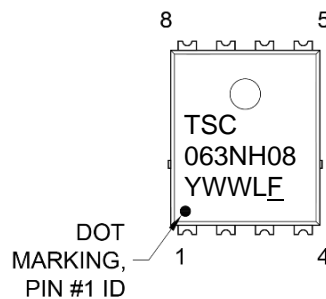
PDFN56U



DETAIL A
(SCALE 2:1)



SUGGESTED PAD LAYOUT
(REFERENCE ONLY)



MARKING DIAGRAM

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PACKAGE OUTLINE REFERENCE: JEITA ED-7500B, EIAJ SC-111BB.
4. MOLDED PLASTIC BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
5. DWG NO. REF: HQ2SD07-PDFN56U-023 REV B.

- 063NH08 = Device marking**
- Y = Year code
 - WW = Week code (01~52)
 - L = Lot code (1~9,A~Z)
 - F = Factory code
 - = AEC-Q101 qualified

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