PerFET™ Power Transistor

FEATURES

- Excellent FOM
- AEC-Q101 Qualified
- Wettable Flank leads for Enhanced AOI
- 100% UIS and Rg tested
- 175°C Operating Junction Temperature
- RoHS Compliant
- Halogen-Free

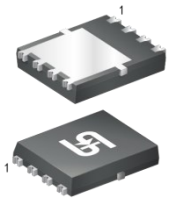
PRODUCT SUMMARY			
PARAMETER		**VALUE**	**UNIT**
V_{DS}		40	V
$R_{DS(on)}$ (max)	V_{GS} = 10V	1.1	mΩ
	V_{GS} = 7V	1.3	
Q_g	V_{GS} = 10V	118	nC

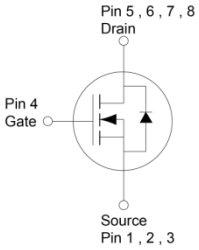
APPLICATIONS

- Automotive Applications
- Solenoid and Motor Drivers
- DC-DC Converters

Pb-Free RoHS COMPLIANT HALOGEN FREE

PDFN56U





Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)				
PARAMETER		**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current, Silicon limited	T_C = 25°C	I_D	323	A
Continuous Drain Current (Note 1)	T_C = 25°C	I_D	175	A
	T_C = 100°C		175	
	T_A = 25°C		40	
Pulsed Drain Current (Note 2,6)		I_{DM}	700	A
Single Pulse Avalanche Current (Note 3)		I_{AS}	59	A
Single Pulse Avalanche Energy (Note 3)		E_{AS}	522	mJ
Total Power Dissipation	T_C = 25°C	P_D	214	W
	T_C = 125°C		71	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +175	°C

THERMAL RESISTANCE			
PARAMETER	**SYMBOL**	**MAXIMUM**	**UNIT**
Thermal Resistance – Junction to Case	$R_{\Theta JC}$	0.7	°C/W
Thermal Resistance – Junction to Ambient (Note 4)	$R_{\Theta JA}$	45	°C/W

Notes:

1. Package current limit.
2. Pulse Width ≤ 100μs.
3. L = 0.3mH, VGS = 10V, RG = 25Ω, Starting TJ = 25°C.
4. Device on a PCB FR4 with 1 in^2 (single layer, 2 oz thick) copper area for drain connection.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)						
PARAMETER	**CONDITIONS**	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 1mA	BV_{DSS}	40	--	--	V
Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	$V_{GS(TH)}$	2.4	2.8	3.6	V
Gate-Source Leakage Current	V_{GS} = ±20V, V_{DS} = 0V	I_{GSS}	--	--	±100	nA
Drain-Source Leakage Current	V_{GS} = 0V, V_{DS} = 40V	I_{DSS}	--	--	1	μA
	V_{GS} = 0V, V_{DS} = 40V T_J = 125°C		--	--	100	
Drain-Source On-State Resistance (Note 5)	V_{GS} = 10V, I_D = 50A	$R_{DS(on)}$	--	0.8	1.1	mΩ
	V_{GS} = 7V, I_D = 50A		--	1	1.3	
Forward Transconductance (Note 5)	V_{DS} = 10V, I_D = 12.5A	g_{fs}	--	85	--	S
Dynamic (Note 6)						
Total Gate Charge	V_{GS} = 7V, V_{DS} = 20V, I_D = 40A	Q_g	--	85	--	nC
Total Gate Charge	V_{GS} = 10V, V_{DS} = 20V, I_D = 40A	Q_g	--	118	--	
Gate-Source Charge		Q_{gs}	--	31	--	
Gate-Drain Charge		Q_{gd}	--	23	--	
Input Capacitance	V_{DS} = 20V, V_{GS} = 0V, f = 1.0MHz	C_{iss}	--	7662	--	pF
Output Capacitance		C_{oss}	--	1751	--	
Reverse Transfer Capacitance		C_{rss}	--	99	--	
Gate Resistance	f = 1.0MHz	R_g	--	1.3	--	Ω
Switching (Note 7)						
Turn-On Delay Time	V_{GS} = 10V, V_{DS} = 20V, I_D = 40A, R_G = 6Ω	$t_{d(on)}$	--	27	--	ns
Rise Time		t_r	--	95	--	
Turn-Off Delay Time		$t_{d(off)}$	--	99	--	
Fall Time		t_f	--	99	--	
Source-Drain Diode						
Diode Forward Voltage (Note 5)	V_{GS} = 0V, I_S = 50A	V_{SD}	--	--	1.1	V
Reverse Recovery Time	I_S = 40A, di/dt = 100A/μs	t_{rr}	--	62	--	ns
Reverse Recovery Charge		Q_{rr}	--	96	--	nC

Notes:

5. Pulse test: Pulse Width ≤ 300μs, duty cycle ≤ 2%.
6. Defined by design. Not subject to production test.
7. Switching time is essentially independent of operating temperature.

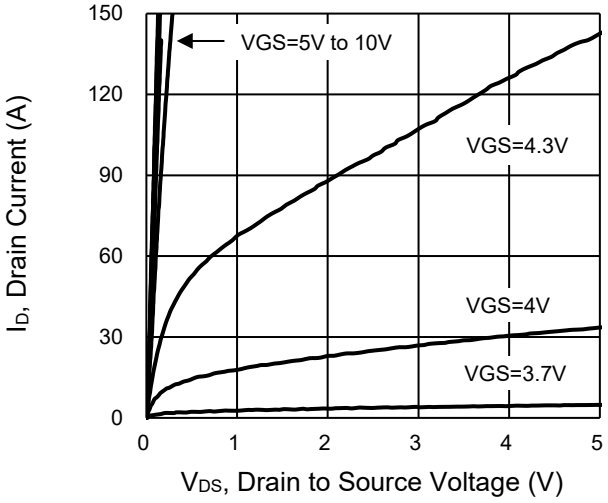
ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TQM011NH04CR RLG	PDFN56U	2,500pcs / 13” Reel

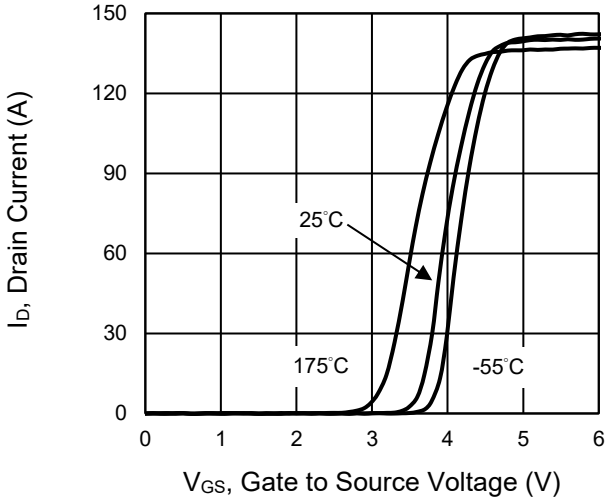
CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

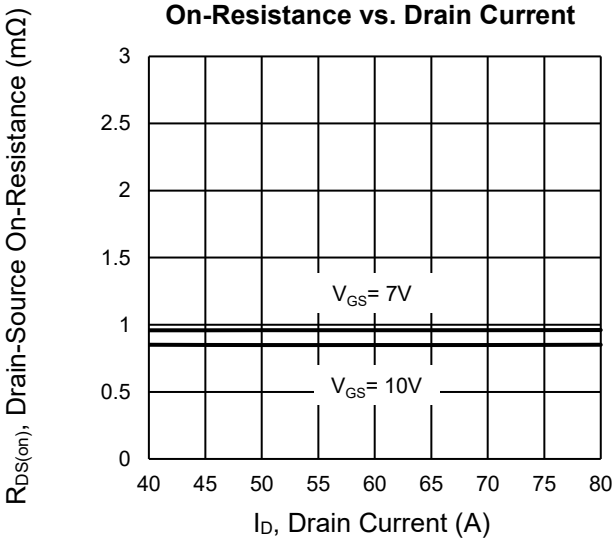
Output Characteristics



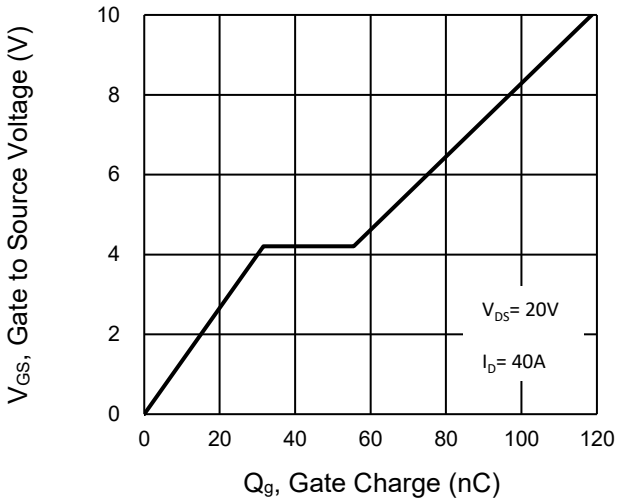
Transfer Characteristics



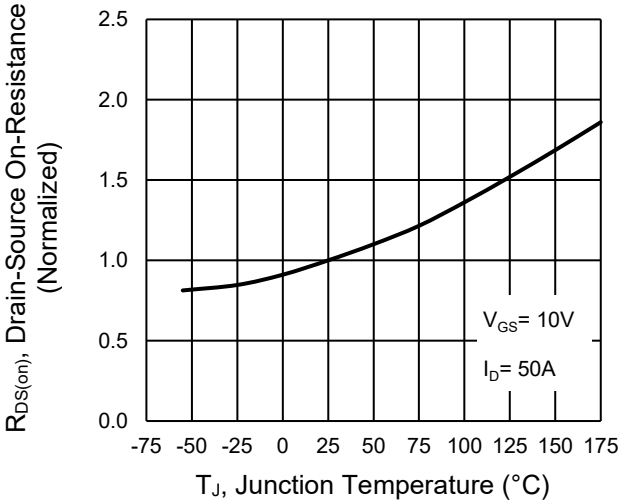
On-Resistance vs. Drain Current



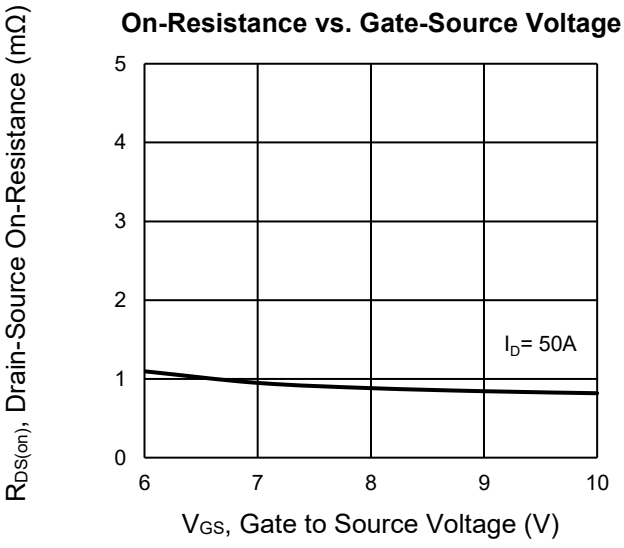
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



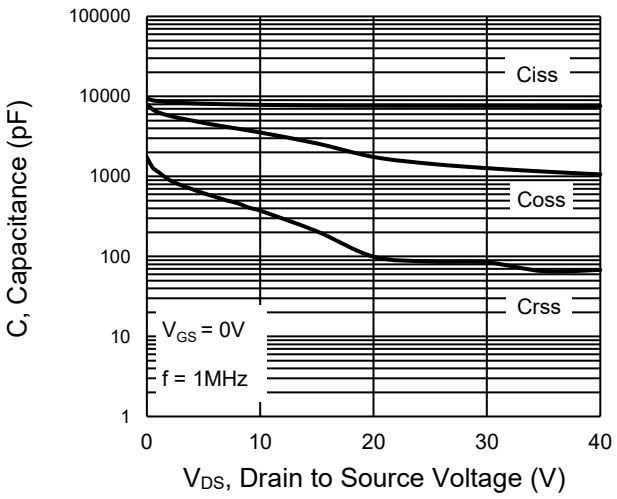
On-Resistance vs. Gate-Source Voltage



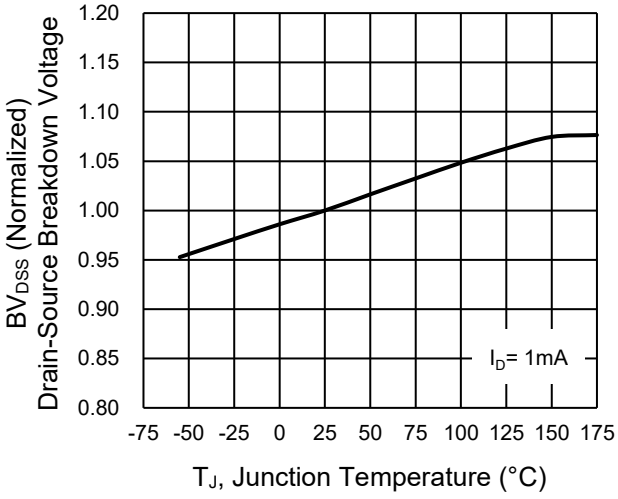
CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

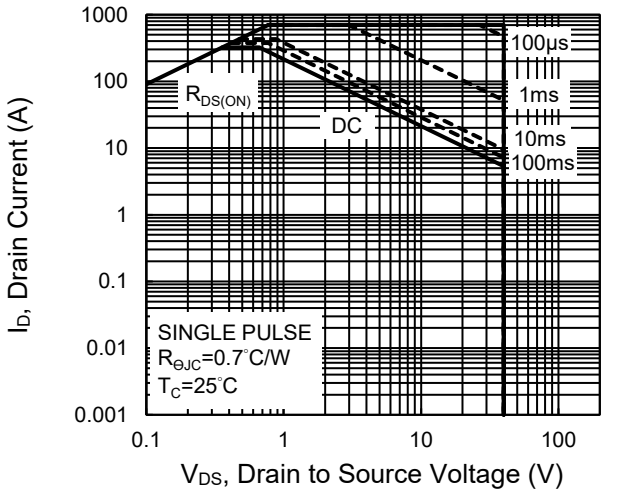
Capacitance vs. Drain-Source Voltage



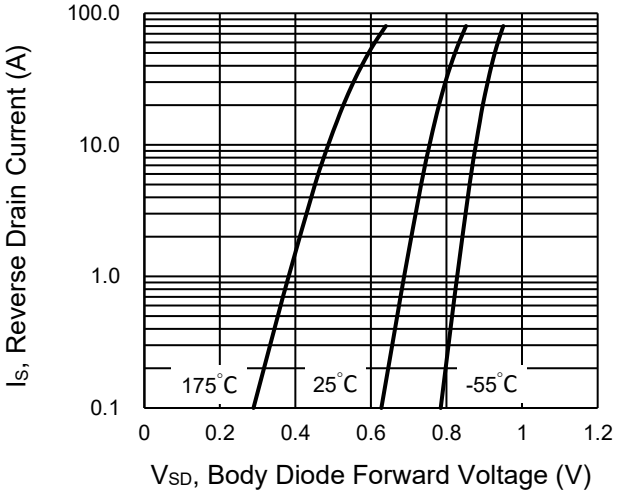
BV_{DSS} vs. Junction Temperature



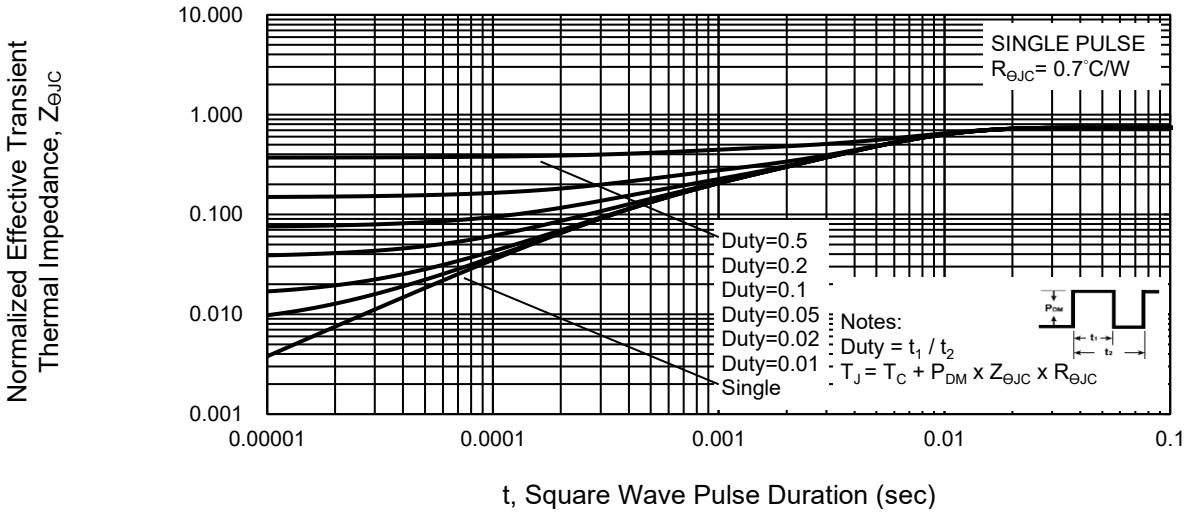
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage



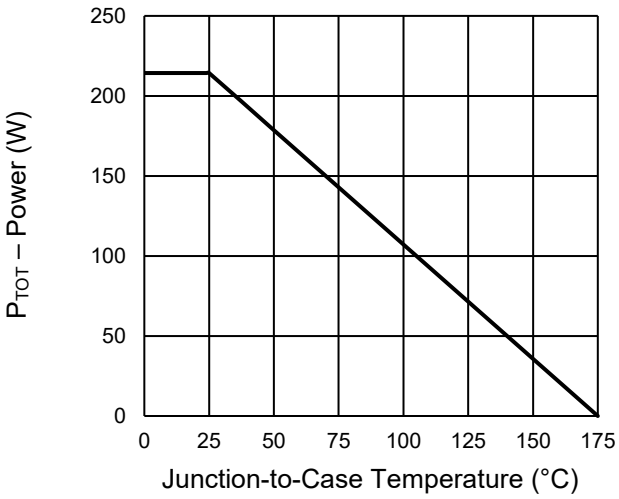
Normalized Thermal Transient Impedance, Junction-to-Case



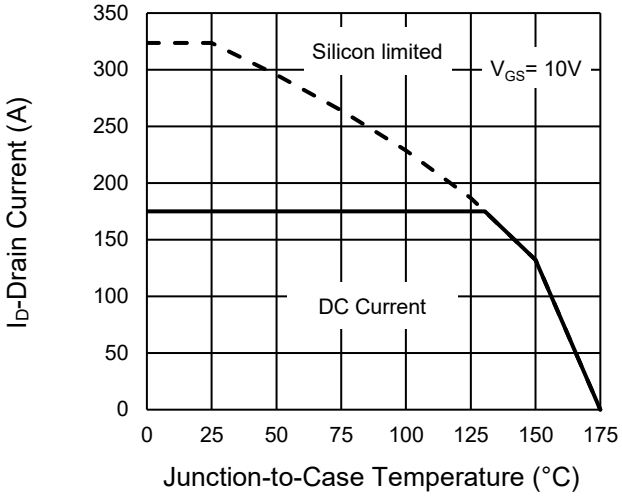
CHARACTERISTICS CURVES

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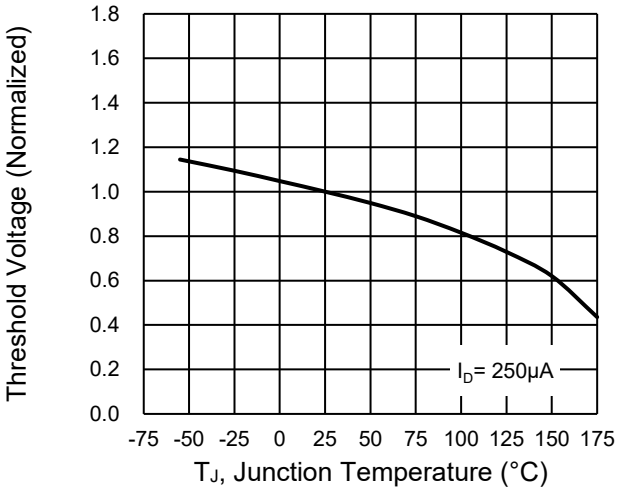
Power Dissipation



Drain Current

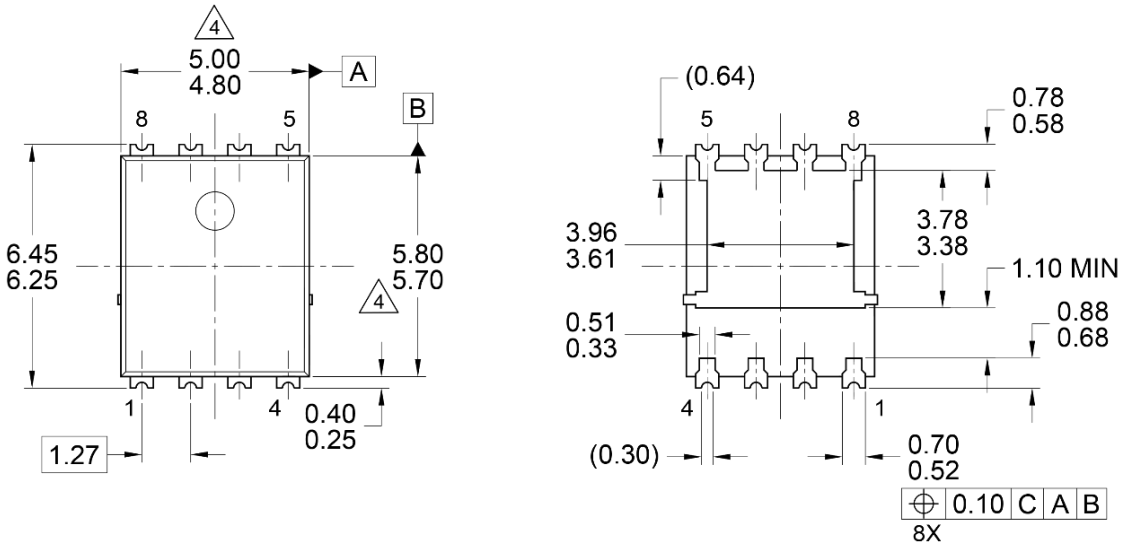


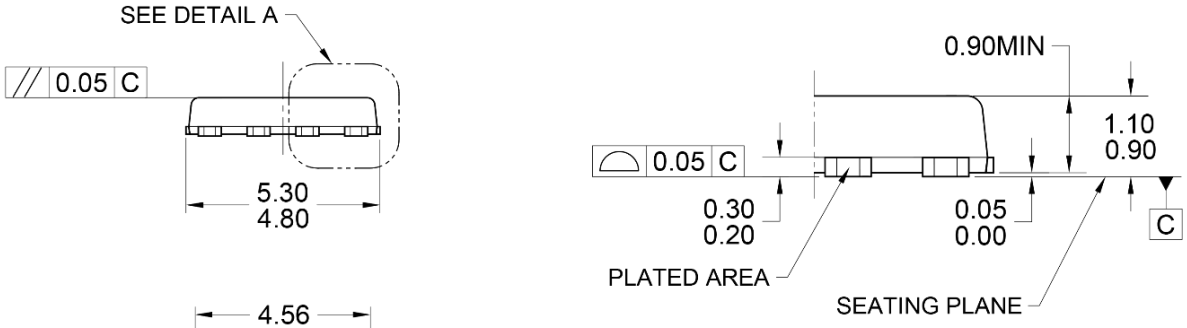
Normalized gate threshold voltage vs Temperature



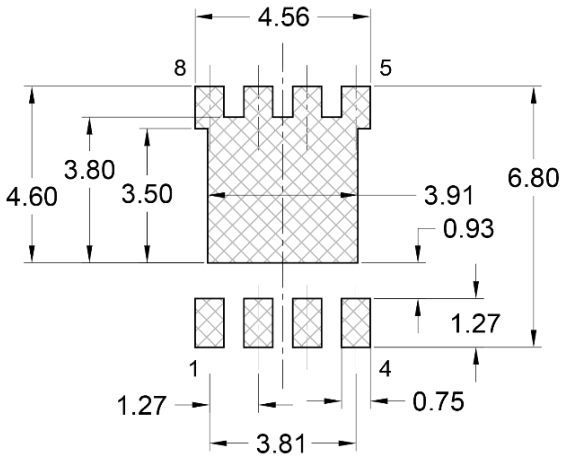
PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

PDFN56U

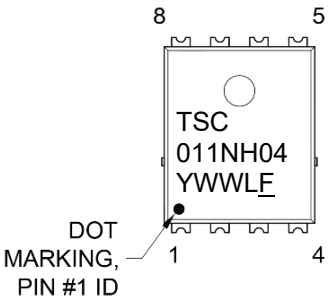




DETAIL A
(SCALE 2:1)



SUGGESTED PAD LAYOUT
(REFERENCE ONLY)



MARKING DIAGRAM

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PACKAGE OUTLINE REFERENCE: JEITA ED-7500B, EIAJ SC-111BB.
4. MOLDED PLASTIC BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
5. DWG NO. REF: HQ2SD07-PDFN56U-023 REV B.

011NH04	= Device marking
Y	= Year code
WW	= Week code (01~52)
L	= Lot code (1~9,A~Z)
F	= Factory code
_	= AEC-Q101 qualified

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