Bi-directional Ultra Low Capacitance ESD Protection Diode

DESCRIPTIONS

The TESDH5V0B05P1Q1 is an ultra-low capacitance TVS (Transient Voltage Suppressor) designed to protect high speed data interfaces. It has been specifically designed to protect sensitive electronic components which are connected to data and transmission lines from over-voltage damage by Electrostatic Discharging (ESD).

TESDH5V0B05P1Q1 incorporates one pair of ultra-low capacitance steering diodes plus a TVS diode. During transient conditions, the steering diodes direct the transient to either the internal ESD line. The internal unique design of clamping cell prevents over-voltage on the data and I/O lines, protecting any downstream components.

The TESDH5V0B05P1Q1 may be used to provide ESD protection up to ±20kV (contact and air discharge) according to IEC61000-4-2, and withstand peak pulse current up to 5.5A (8/20μs) according to IEC61000-4-5.

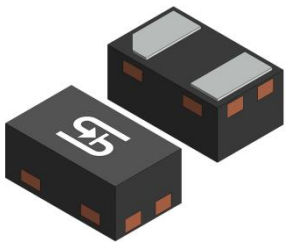
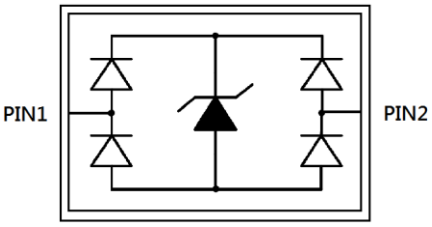
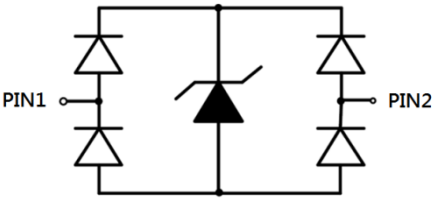
FEATURES

- ESD protect for 1 line with bidirectional
- Provide ESD protection for each channel to IEC61000-4-2 (ESD) ±20kV (air), ±20kV (contact) IEC61000-4-5 (Lightning) 5.5A (8/20μs)
- Protect one I/O line
- Fast turn-on and Low clamping voltage
- Solid-state silicon-avalanche and active circuit triggering technology
- Suitable for 5V and below, operating voltage applications
- Ultra-low capacitance: C_J = 0.40pF(typ.)
- Ultra-low leakage current: I_R = 2nA(typ.)
- Low clamping voltage: V_{CL} = 9.8V(typ.) @ I_{TLP} = 16A
- Moisture sensitivity level: level 1, per J-STD-020
- RoHS Compliant
- Halogen-Free according to IEC61249-2-21

APPLICATION

- USB 2.0 and USB 3.0
- HDMI 1.3 and HDMI 1.4
- SATA and eSATA
- DVI
- IEEE 1394
- PCI Express
- Portable Electronics
- Notebooks

Pb-Free RoHS COMPLIANT HALOGEN FREE

PACKAGE: DFN1006-2L	PIN CONFIGURATION	CIRCUIT DIAGRAM
		

PIN 1	Cathode 1
PIN 2	Cathode 2

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)			
PARAMETER	**SYMBOL**	**VALUE**	**UNIT**
Peak pulse power (tp = 8/20us)	P_{PK}	46	W
Peak pulse current (tp = 8/20us)	I_{PP}	5.5	A
ESD according to IEC61000-4-2 air discharge	V_{ESD}	±20	kV
ESD according to IEC61000-4-2 contact discharge		±20	kV
Junction temperature	T_J	125	°C
Operating temperature range	T_{OP}	-40 to +85	°C
Storage temperature range	T_{STG}	-55 to +150	°C

ELECTRICAL SPECIFICATIONS (T_A = 25°C unless otherwise noted)						
PARAMETER	**CONDITIONS**	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
Reverse working voltage		V_{RWM}	-	-	5	V
Reverse breakdown voltage	I_R = 1mA, T_J = 25°C	V_{BR}	7	-	12.5	V
Reverse leakage current	V_{RWM} = 5V	I_R	-	2	50	nA
Clamping voltage(1)	I_{PP} = 1.0A, tp = 8/20us	V_C	-	-	5.5	V
	I_{PP} = 5.5A, tp = 8/20us		-	-	8.5	V
Clamping voltage(2)	I_{TLP} = 16A, tp = 100ns	V_{CL}	-	9.8	-	V
Junction capacitance	f = 1MHz, V_R = 0V	C_J	-	0.4	0.5	pF
Dynamic resistance(2)		R_{DYN}	-	0.37	-	Ω

Notes:

1. Non-repetitive current pulse, according to IEC61000-4-5.
2. TLP parameter: Z_0 = 50 Ω, tp = 100ns, tr = 2ns, averaging window from 60ns to 80ns. RDYN is calculated from 4A to 16A.

ORDERING INFORMATION		
ORDERING CODE	**PACKAGE**	**PACKING**
TESDH5V0B05P1Q1 M5G	DFN1006-2L	10,000 / 7" Tape & Reel

CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

Fig.1 Peak Pulse Power vs. Junction Temperature

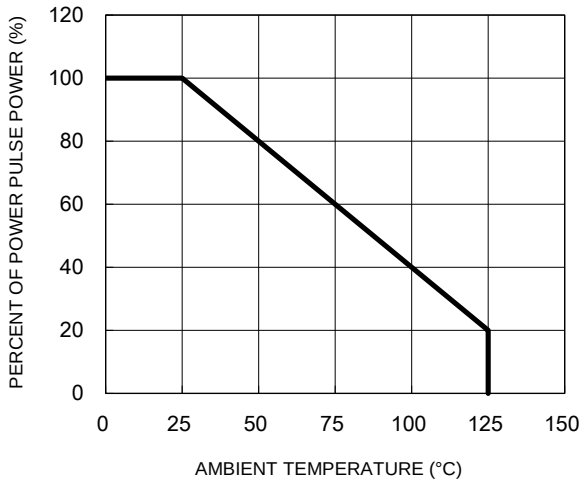


Fig.2 Non-Repetitive Peak Pulse Power vs. Pulse Time

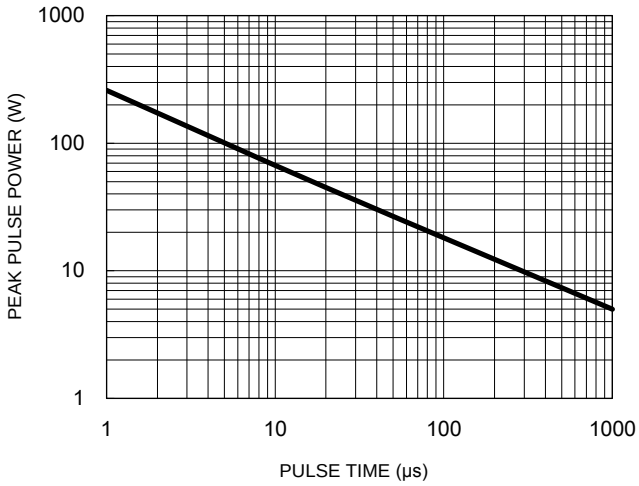


Fig.3 Clamping Voltage vs. Peak Pulse Current

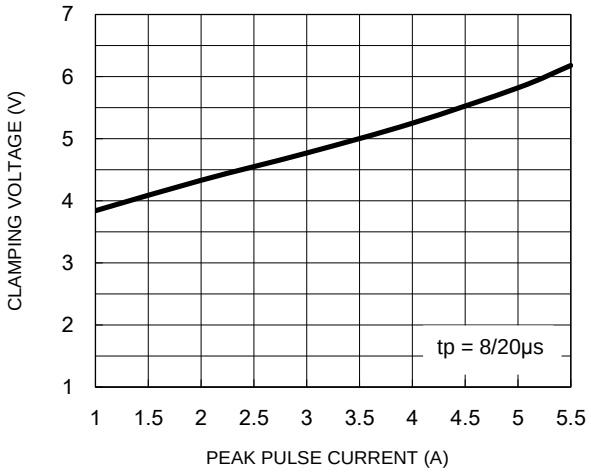


Fig.4 Capacitance vs. Reverse Voltage

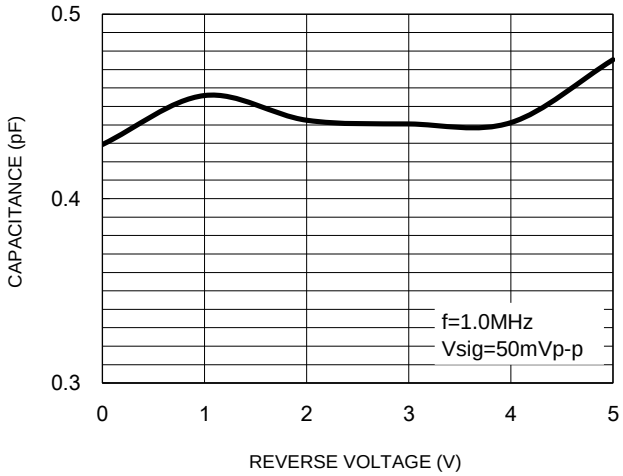
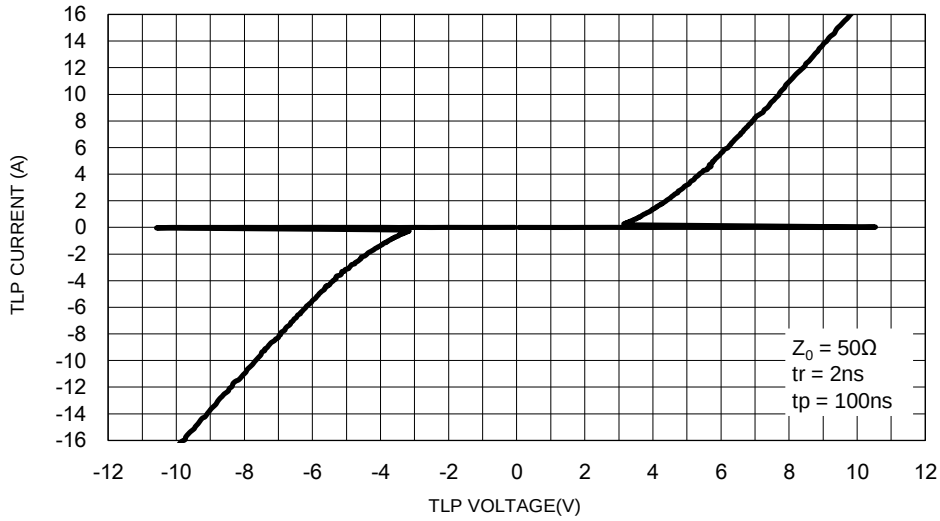


Fig.5 TLP Curve



CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

Fig.6 8/20μs pulse waveform per IEC61000-4-5

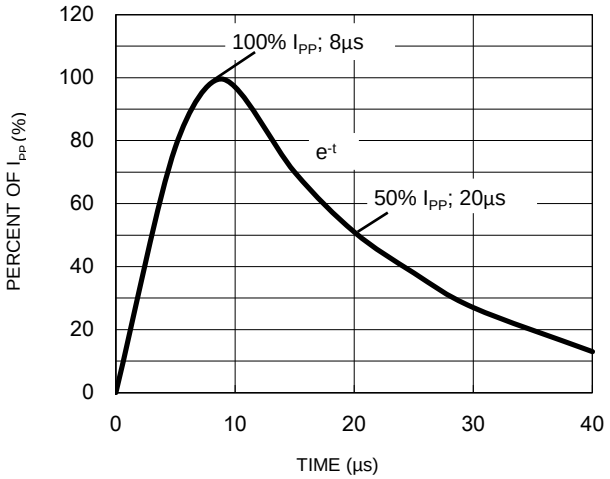
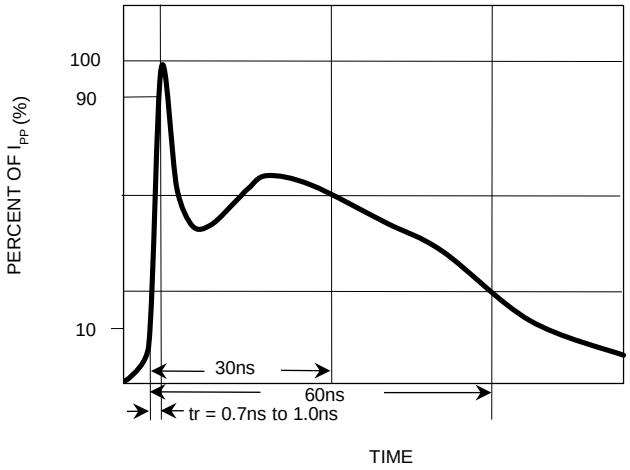


Fig.7 ESD pulse waveform per IEC61000-4-2



APPLICATION INFORMATION

Device Connection

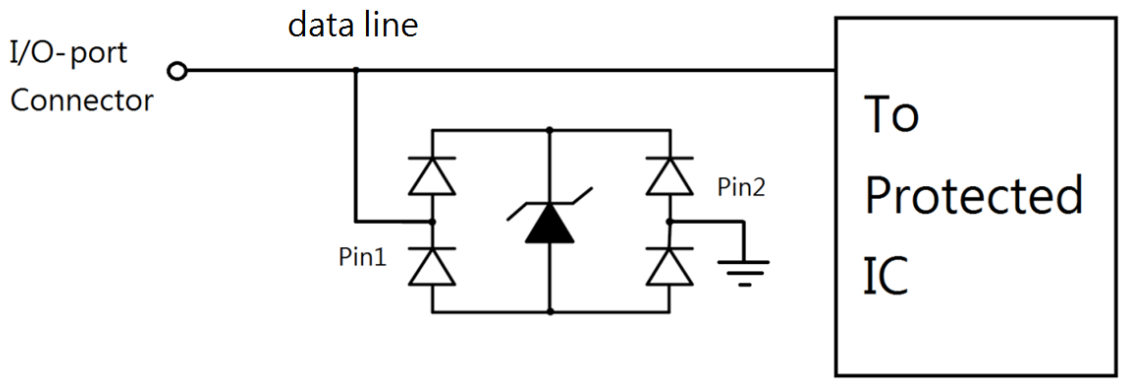
The TESDH5V0B05P1Q1 is designed to protect one data lines from transient over-voltage (such as ESD stress pulse). It provides bidirectional protection.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus, the following guidelines are recommended:

- Let the path length between the protected lines and the TESDH5V0B05P1Q1 minimize.
- Place the TESDH5V0B05P1Q1 near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.

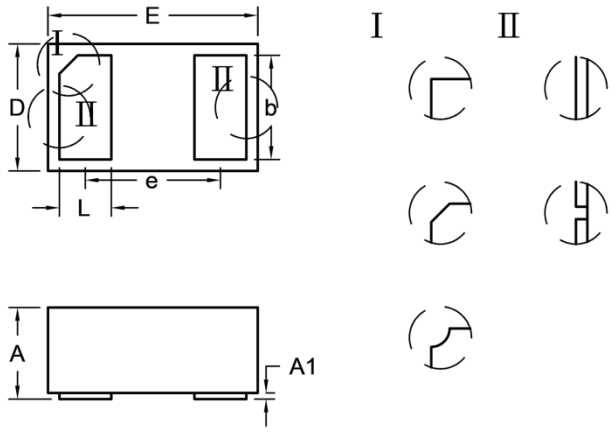
The Fig.1 below shown the onnection for data line ESD protection

Fig.1 ESD protection by TESDH5V0B05P1Q1



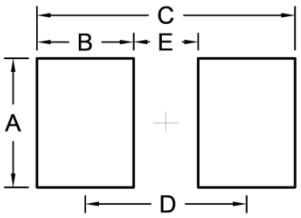
PACKAGE OUTLINE DIMENSIONS

DFN1006-2L



DIM.	Unit (mm)		Unit (inch)	
	Min.	Max.	Min.	Max.
A	0.34	0.53	0.013	0.021
A1	0.00	0.05	0.000	0.002
b	0.45	0.55	0.018	0.022
D	0.55	0.675	0.022	0.027
E	0.95	1.075	0.037	0.042
e	0.65		0.026	
L	0.20	0.30	0.008	0.012

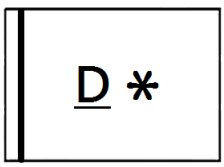
SUGGESTED PAD LAYOUT



Symbol	Unit (mm)	Unit (inch)
A	0.60	0.024
B	0.45	0.018
C	1.20	0.047
D	0.75	0.030
E	0.30	0.012

Notes:
This recommended land pattern is for reference purposes only. Please consult your manufacturing group to ensure your PCB design guidelines are met.

MARKING DIAGRAM



D = Device Code
* = Month Code (A - Z)

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