

Bi-directional ESD Protection Diode

DESCRIPTIONS

The TESDH5V0B03P1Q0 is Bidirectional ESD rated clamping cell to protect power interfaces, or one control line, or one low speed data line in an electronic system. It has been specifically designed to protect sensitive electronic components which are connected to power and control lines from over-voltage damage by Electrostatic Discharging (ESD), and Lightning.

TESDH5V0B03P1Q0 is a unique design which includes proprietary clamping cells in a small package. During transient conditions, the proprietary clamping cells prevent over-voltage on the control/data/power lines, protecting any downstream components.

The TESDH5V0B03P1Q0 may be used to provide ESD protection up to $\pm 30\text{kV}$ (contact and air discharge) according to IEC61000-4-2, and withstand peak pulse current up to 4.5A (8/20 μs) according to IEC61000-4-5


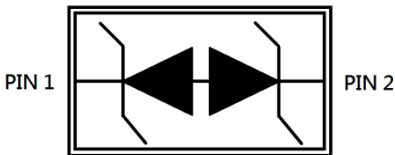
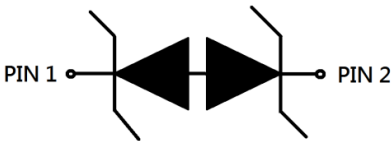
FEATURES

- ESD protect for 1 line with bidirectional.
- Provide ESD protection for each channel to IEC61000-4-2 (ESD) $\pm 20\text{kV}$ (air), $\pm 20\text{kV}$ (contact) IEC61000-4-5 (Lightning) 4.5A (8/20 μs)
- Suitable for 5V and below, operating voltage applications
- Ultra small package saves board space.
- Protect one I/O line or one power line.
- Moisture sensitivity level: level 1, per J-STD-020
- RoHS Compliant
- Halogen-Free

APPLICATION

- SATA and eSATA
- PCI Express
- Notebooks
- USB3.1 and USB3.0 interfaces
- USB Type-C interface
- DisplayPort interface



PACKAGE: DFN0603-2L	PIN CONFIGURATION	CIRCUIT DIAGRAM
		

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)			
PARAMETER	SYMBOL	VALUE	UNIT
Peak pulse power ($t_p = 8/20\mu\text{s}$)	P_{PK}	100	W
Peak pulse current ($t_p = 8/20\mu\text{s}$)	I_{PP}	4.5	A
ESD according to IEC61000-4-2 air discharge	V_{ESD}	± 20	kV
ESD according to IEC61000-4-2 contact discharge		± 20	kV
Junction temperature range	T_J	-55 to +125	$^\circ\text{C}$
Storage temperature range	T_{STG}	-55 to +150	$^\circ\text{C}$

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Reverse working voltage		V_{RWM}	-	-	5	V
Reverse breakdown voltage	$I_R = 1\text{mA}$, $T_J = 25^\circ\text{C}$	V_{BR}	6	-	9.5	V
Reverse leakage current	$V_{RWM} = 5\text{V}$	I_R	-	-	50	nA
Clamping voltage ⁽¹⁾	$I_{PP} = 4.5\text{A}$, $t_p = 8/20\mu\text{s}$	V_C	-	-	22	V
Clamping voltage ⁽²⁾	$I_{TLP} = 4\text{A}$, $t_p = 100\text{ns}$	V_{CL}	-	16	-	V
	$I_{TLP} = 16\text{A}$, $t_p = 100\text{ns}$		-	32	-	V
Junction capacitance	1MHz, $V_R = 0\text{V}$	C_J	-	0.20	0.35	pF
Dynamic resistance ⁽²⁾		R_{DYN}	-	1.33	-	Ω

Notes:

1. Non-repetitive current pulse, according to IEC61000-4-5.
2. TLP parameter: $Z_0 = 50\ \Omega$, $t_p = 100\text{ns}$, $t_r = 2\text{ns}$, averaging window from 60ns to 80ns. R_{DYN} is calculated from 4A to 16A.

ORDERING INFORMATION		
ORDERING CODE	PACKAGE	PACKING
TESDH5V0B03P1Q0 M3G	DFN0603-2L	10,000 / 7" Reel

CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Fig.1 Peak Pulse Power vs. Junction Temperature **Fig.2 Non-Repetitive Peak Pulse Power vs. Pulse Time**

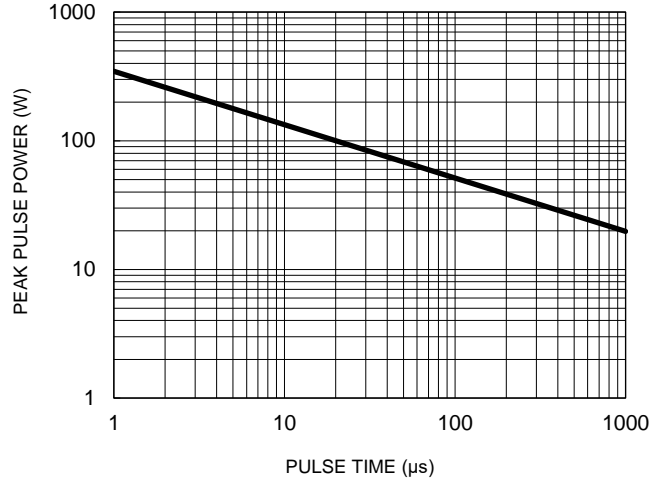
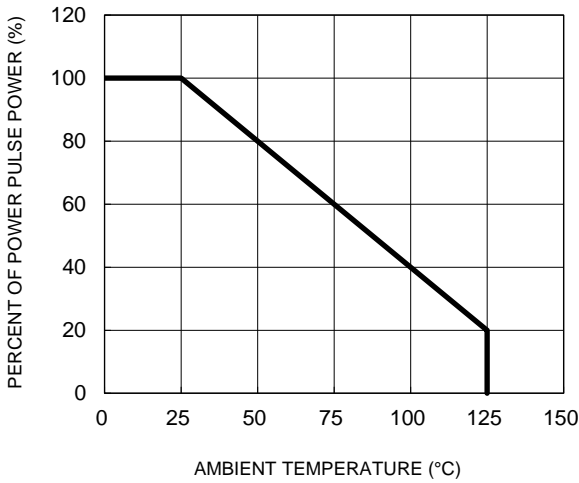


Fig.3 Clamping Voltage vs. Peak Pulse Current

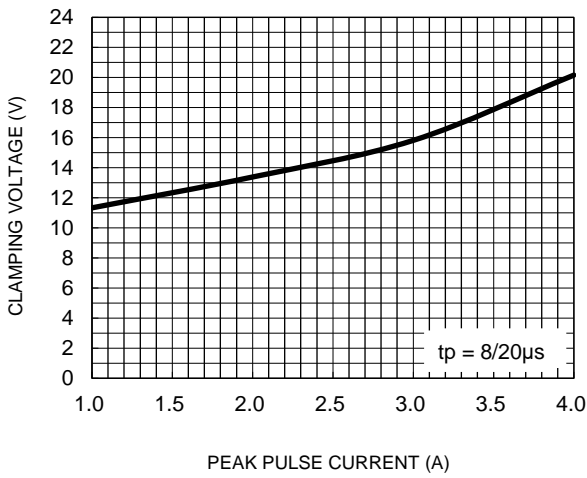


Fig.4 Capacitance vs. Reverse Voltage

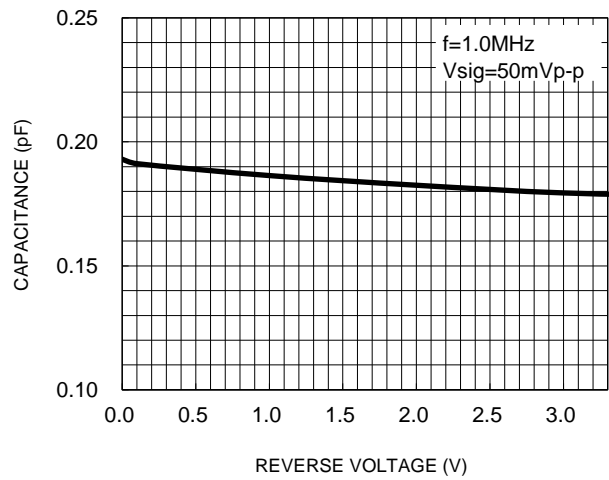
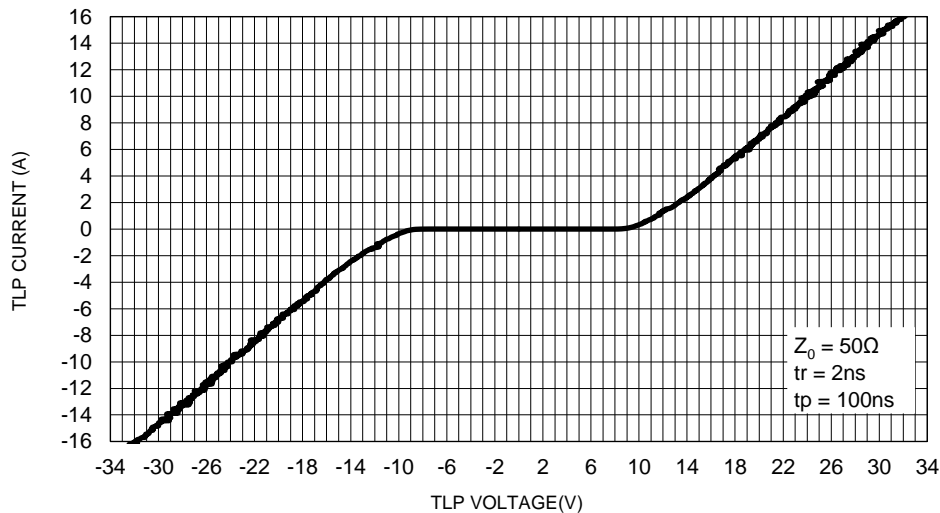


Fig.5 TLP Curve



CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Fig.6 8/20 μs pulse waveform per IEC61000-4-5

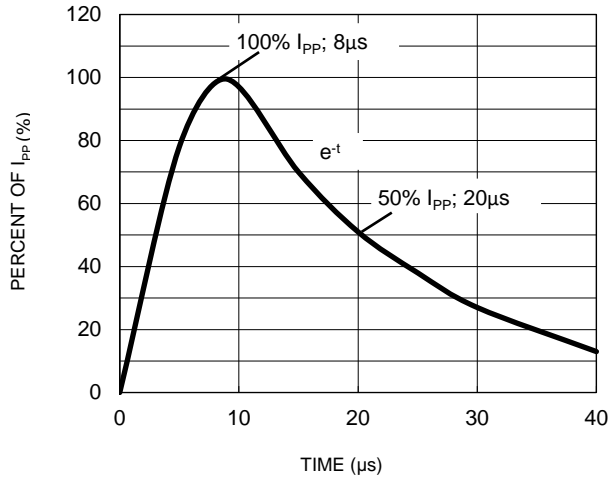
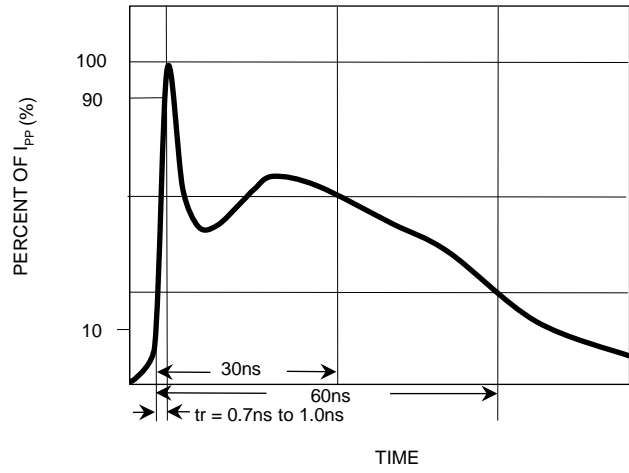


Fig.7 ESD pulse waveform per IEC61000-4-2



APPLICATION INFORMATION

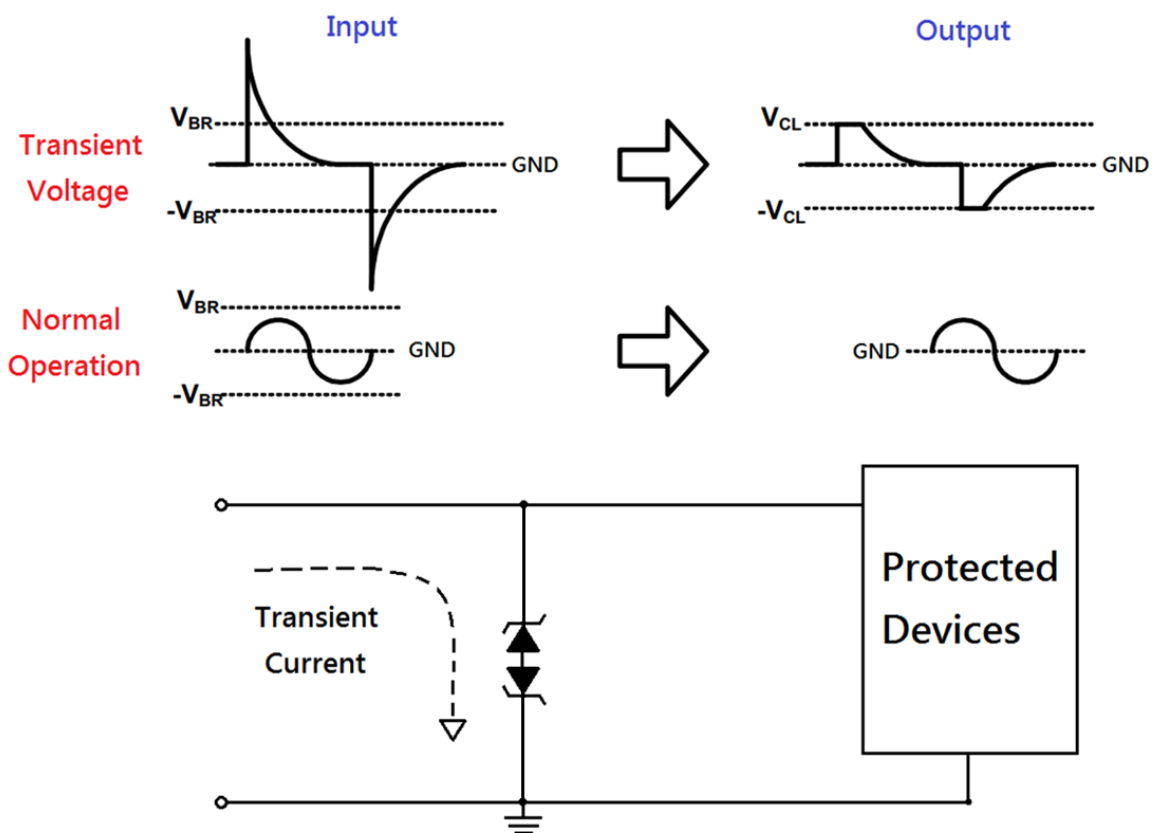
Device Connection

The TESDH5V0B03P1Q0 is designed to protect one line against system ESD Lightning pulses by clamping it to an acceptable reference. It provides bidirectional protection. The usage of the TESDH5V0B03P1Q0 is shown in Fig1. Protected line, such as data line, control line, or power line. In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of TESDH5V0B03P1Q0 should be kept as short as possible.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus, the following guidelines are recommended:

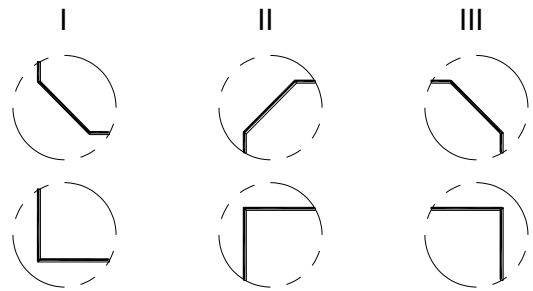
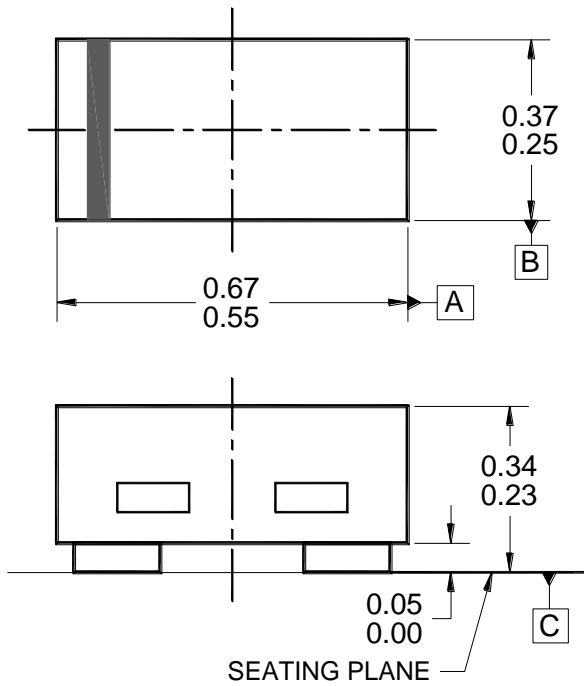
- Let the path length between the protected lines and the TESDH5V0B03P1Q0 minimize.
- Place the TESDH5V0B03P1Q0 near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.

Fig.1 ESD protection by TESDH5V0B03P1Q0

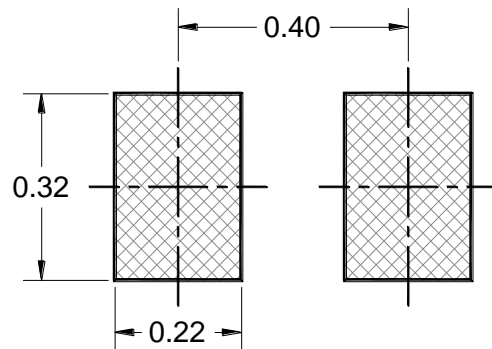
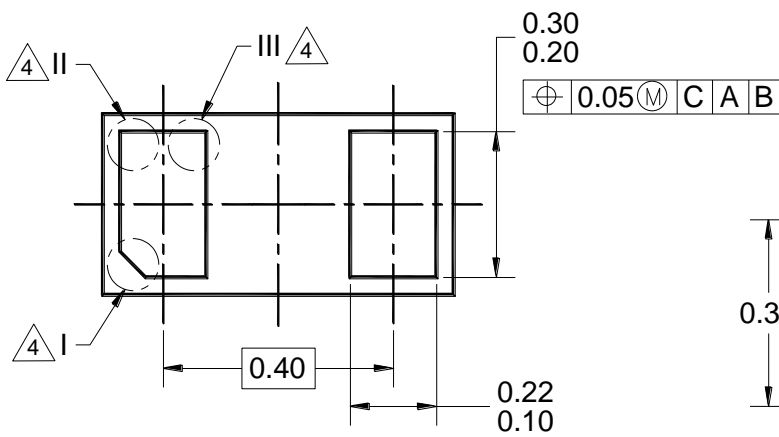


PACKAGE OUTLINE DIMENSIONS

DFN0603-2L



CATHODE TERMINAL CORNER NOTCH OPTION



SUGGESTED PAD LAYOUT



MARKING DIAGRAM

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PACKAGE SIZE CODE REFERENCE:
EIA (inch) NAME: 0201 (0.024in x 0.012in)
IEC (metric) NAME: 0603 (0.6mm x 0.3mm)
4. CATHODE TERMINAL MAY HAVE CHAMFER NOTCH OR FULL 90 DEGREES CORNER.
5. DWG NO. REF: HQ2SD07-DFN0603-067 REV B.

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