Uni-directional ESD Protection Diode

DESCRIPTIONS

The TESDA26VU55P2Q3 is Uni-directional ESD rated clamping cell to protect power interfaces, or control line, or low speed data line in an electronic system. It has been specifically designed to protect sensitive electronic components which are connected to power and control lines from over-voltage damage by Electrostatic Discharging (ESD), and Lightning.

ESD protection device in a small DNF1010 Surface-Mounted Device (SMD) plastic package designed to protect two automotive In-vehicle network bus lines from the damage caused by Electrostatics discharge (ESD) and other transients.

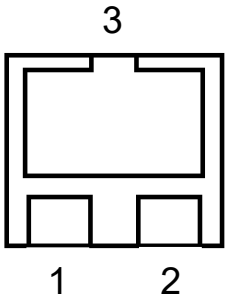
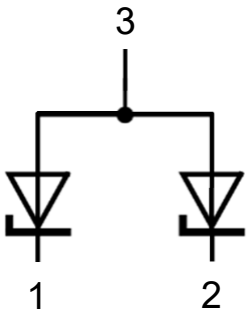
The TESDA26VU55P2Q3 may be used to provide ESD protection up to ±15kV (air), ±30kV (contact) according to IEC61000-4-2, and withstand peak pulse current up to 0.87A(10/1000μs) according to IEC61643-321.

FEATURES

- AEC-Q101 qualified
- ESD protect for 2 lines with unidirectional.
- Provide ESD protection for each channel to IEC61000-4-2 (ESD) ±15kV (air), ±30kV(contact)
- IEC61643-321 0.87A (10/1000μs)
- Suitable for 26V and below, operating voltage applications
- Protect I/O line or power line.
- Moisture sensitivity level: level 1, per J-STD-020
- RoHS Compliant
- Halogen-Free

APPLICATION

- Portable electronics
- Computers and peripherals
- Smartphones and accessories

PACKAGE: DFN1010-3LW	PIN CONFIGURATION	CIRCUIT DIAGRAM
		

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)			
PARAMETER	**SYMBOL**	**VALUE**	**UNIT**
Peak pulse power (tp = 10/1000us)	P_{PK}	40	W
Peak pulse current (tp = 10/1000us)	I_{PP}	0.87	A
ESD according to IEC61000-4-2 air discharge	V_{ESD}	±15	kV
ESD according to IEC61000-4-2 contact discharge		±30	kV
Junction temperature range	T_J	-55 to +150	°C
Storage temperature range	T_{STG}	-55 to +150	°C

ELECTRICAL SPECIFICATIONS (T_A = 25°C unless otherwise noted)						
PARAMETER	**CONDITIONS**	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
Reverse working voltage		V_{RWM}	-	-	26	V
Forword voltage	I_F = 10mA, T_J = 25°C	V_F	-	-	0.9	V
Reverse breakdown voltage	I_R = 1mA, T_J = 25°C	V_{BR}	31.35	32.8	34.65	V
Reverse leakage current	V_{RWM} = 26V	I_R	-	0.5	5	nA
Clamping voltage(1)	I_{PP} = 0.87A, tp = 10/1000μs	V_C	-	-	46	V
Clamping voltage(2)	I_{TLP} = 4A, tp = 100ns	V_{CL}	-	35.1	-	V
	I_{TLP} = 16A, tp = 100ns		-	39.9	-	V
Junction capacitance	1MHz, V_R = 0V	C_J	-	49.5	55	pF
Dynamic resistance(2)		R_{DYN}	-	0.4	-	Ω

Notes:

1. Non-repetitive current pulse, according to IEC61643-321.
2. TLP parameter: Z_0 = 50 Ω, tp = 100ns, tr = 2ns, averaging window from 60ns to 80ns. R_{DYN} is calculated from 4A to 16A.

ORDERING INFORMATION		
ORDERING CODE	**PACKAGE**	**PACKING**
TESDA26VU55P2Q3 RNG	DFN1010-3LW	10,000 / 7” Tape & Reel

CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

Fig.1 Peak Pulse Power vs. Junction Temperature

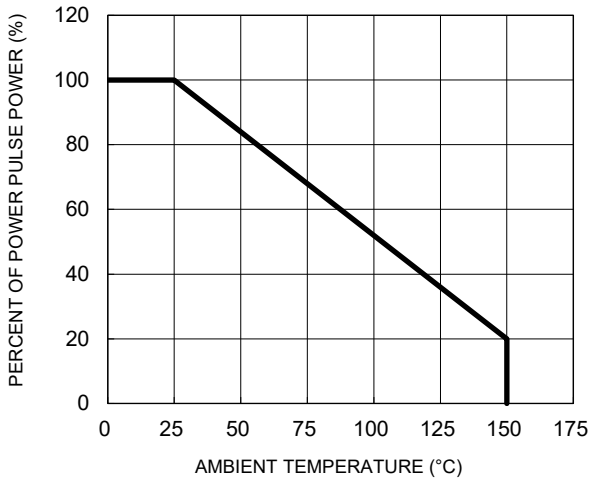


Fig.2 Non-Repetitive Peak Pulse Power vs. Pulse Time

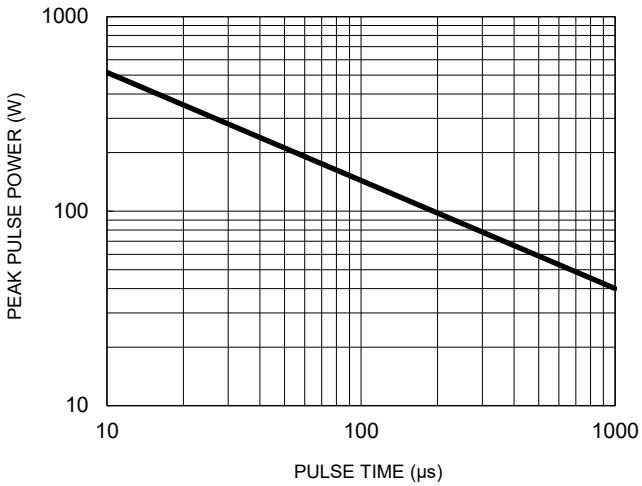


Fig.3 Clamping Voltage vs. Peak Pulse Current

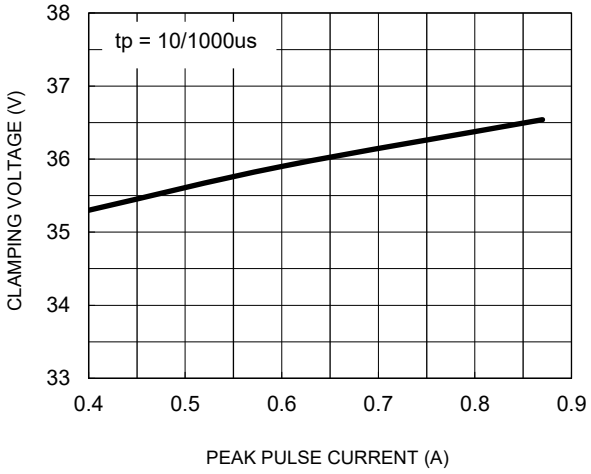


Fig.4 Capacitance vs. Reverse Voltage

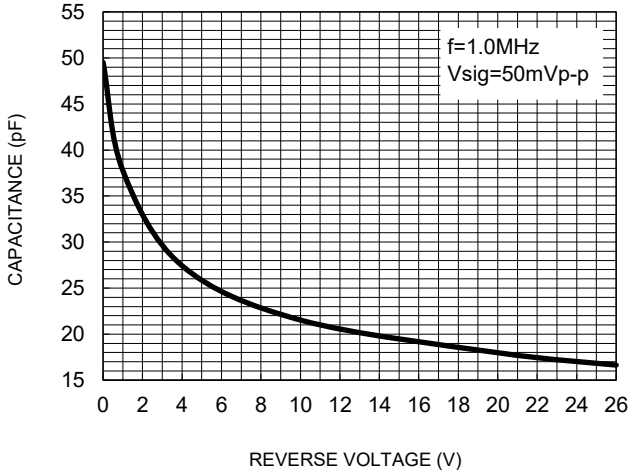
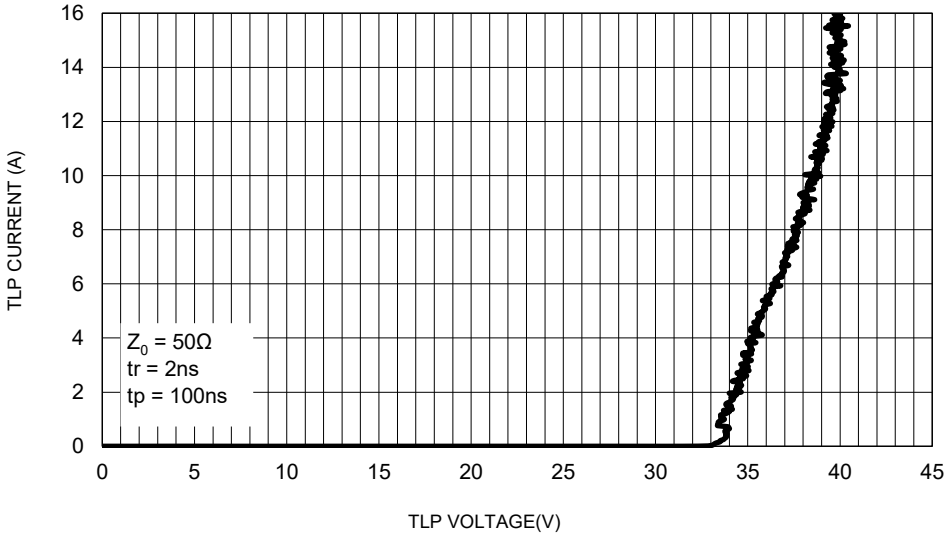


Fig.5 TLP Curve



CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

Fig.6 10/1000μs pulse waveform

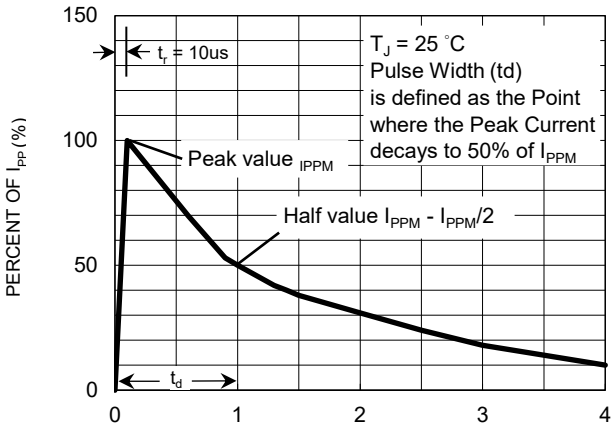
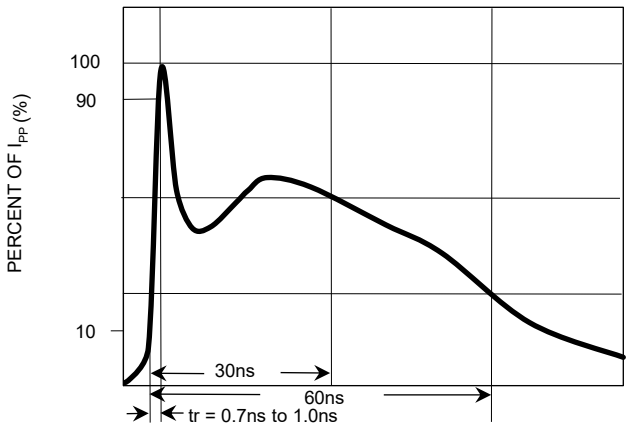


Fig.7 ESD pulse waveform per IEC61000-4-2



APPLICATION INFORMATION

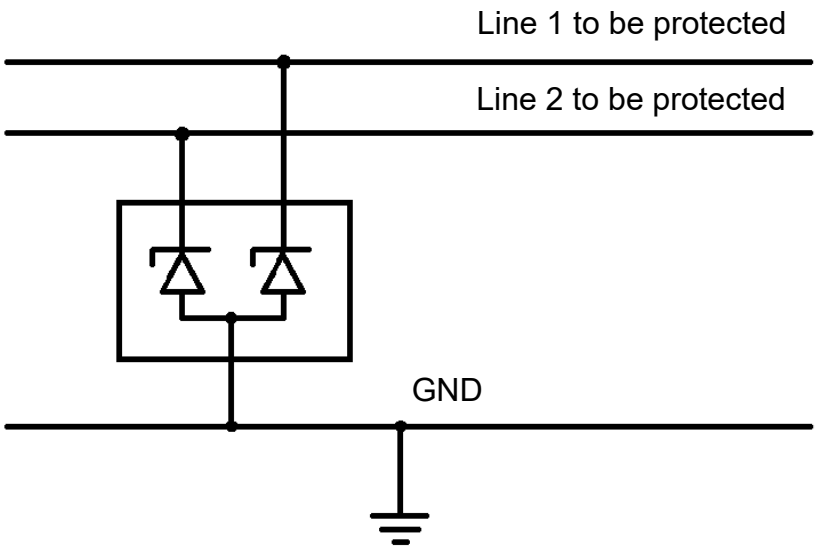
Device Connection

The TESDA26VU55P2Q3 is designed for protection from the damage caused by ESD and surge pulses. The usage of the TESDA26VU55P2Q3 is shown in Fig1.Protected line.
To minimize parasitic inductance in the board traces, all path lengths connected to the pins of TESDA26VU55P2Q3 should be kept as short as possible.

To obtain enough suppression of ESD transient, a good circuit board is critical. Thus, the following guidelines are recommended:

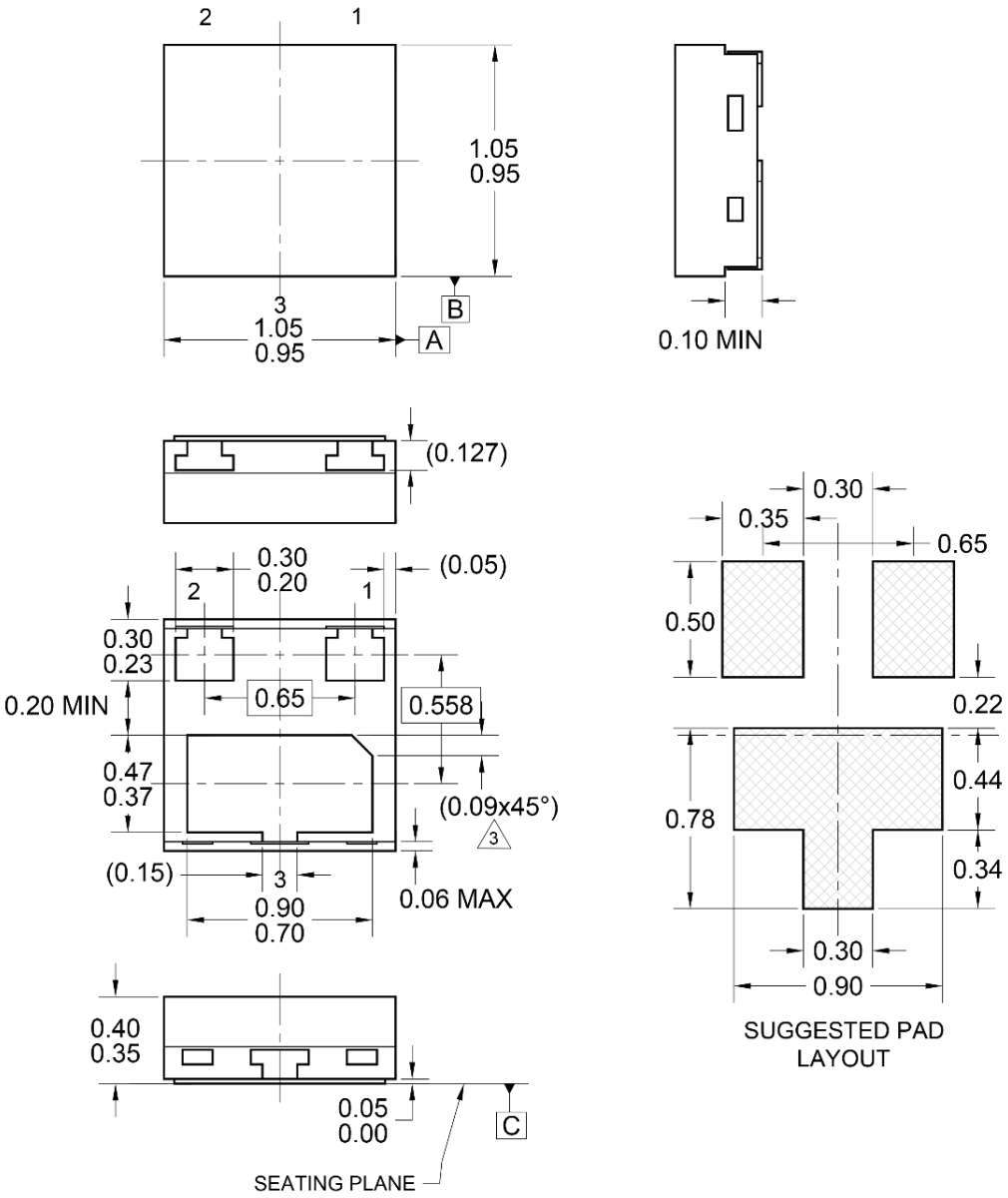
- Let the path length between the protected lines and the TESDA26VU55P2Q3 minimize.
- Place the TESDA26VU55P2Q3 near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground plane whenever possible.

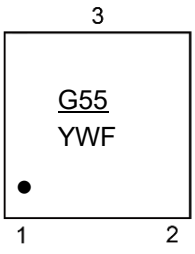
Fig.1 ESD protection by TESDA22VU60P2Q3



PACKAGE OUTLINE DIMENSIONS

DFN1010-3LW





MARKING DIAGRAM

F60 = Device code
Y = Year code
W = Bi-week code (A~Z)
F = Factory code

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. LARGE TERMINAL PAD WITH CHAMFER CORNER IS A COMMON ANODE TERMINAL.
4. PACKAGE OUTLINE REFERENCE: JEDEC MO-340BA.
5. DWG NO. REF: HQ2SD07-DFN1010_3LW-124 REV B.

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