Taiwan Semiconductor

30mA, 40V Low V_F SMD Schottky Barrier Diode

FEATURES

- Low power loss, high current capability, low V_F
- Surface mount device type
- Moisture sensitivity level: level 1, per J-STD-020
- RoHS Compliant

APPLICATIONS

- Switching mode power supply (SMPS)
- Adapters
- Lighting application
- On-board DC/DC converter

MECHANICAL DATA

- Case: SOD-323F
- Molding compound meets UL 94V-0 flammability rating
- Terminal: Matte tin plated leads, solderable per J-STD-002
- Meet JESD 201 class 1A whisker test
- Polarity: Indicated by cathode band
- Weight: 4.60mg (approximately)

KEY PARAMETERS			
PARAMETER	R VALUE UNI		
I _F	30	mA	
V _{RRM}	40	V	
V _F at I _F = 1mA	0.37	V	
T _{J MAX}	125	°C	
Package	SOD-323F		
Configuration	Single die		









ABSOLUTE MAXIMUM RATINGS (T _A = 25°C unless otherwise noted)				
PARAMETER		SYMBOL	RB751V-40WS	UNIT
Marking code on the device			S8	
Power Dissipation		P _D	200	mW
Repetitive Peak Reverse Voltage		V _{RRM}	40	V
Reverse Voltage		V _R	30	V
Forward current		I _F	30	mA
Non-repetitive peak forward surge current	60Hz for 1 Cyc.	I _{FSM}	0.2	А
Junction temperature range		TJ	-40 to +125	°C
Storage temperature range		T _{STG}	-40 to +125	°C



THERMAL PERFORMANCE			
PARAMETER	SYMBOL	ТҮР	UNIT
Junction-to-ambient thermal resistance	R _{eja}	500	°C/W

ELECTRICAL SPECIFICATIONS (T _A = 25°C unless otherwise noted)					
PARAMETER	CONDITIONS	SYMBOL	ТҮР	MAX	UNIT
Forward Voltage ⁽¹⁾	I _F = 1mA	V _F	-	0.37	V
Reverse current @ rated $V_R^{(2)}$	V _R = 30V	I _R	-	0.50	μA
Junction capacitance	$1MHz, V_R = 1V$	CJ	2	-	pF

Notes:

1. Pulse test with PW = 0.3ms

2. Pulse test with PW = 30ms

ORDERING INFORMATION			
ORDERING CODE ⁽¹⁾	PACKAGE	PACKING	
RB751V-40WS RR	SOD-323F	3K / 7" Reel	
RB751V-40WS RRG	SOD-323F	3K / 7" Reel	
RB751V-40WS R9	SOD-323F	10K / 13" Reel	
RB751V-40WS R9G	SOD-323F	10K / 13" Reel	

Notes:

1. "G" means green compound (halogen-free according to IEC 61249-2-21)



CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

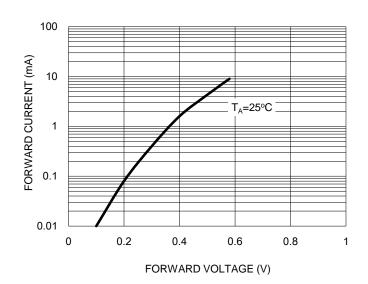


Fig.1 Typical Forward Characteristics

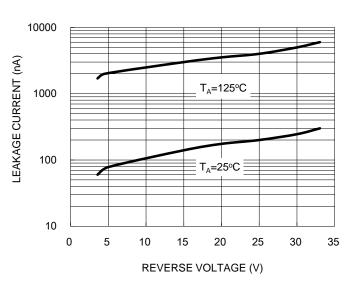


Fig.2 Typical Reverse Characteristics

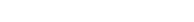


Fig.3 Typical Junction Capacitance

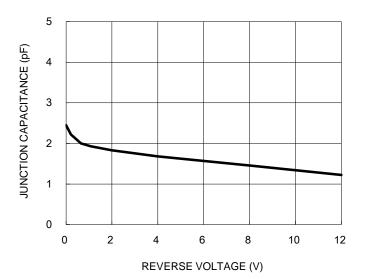
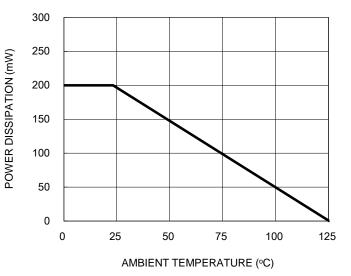
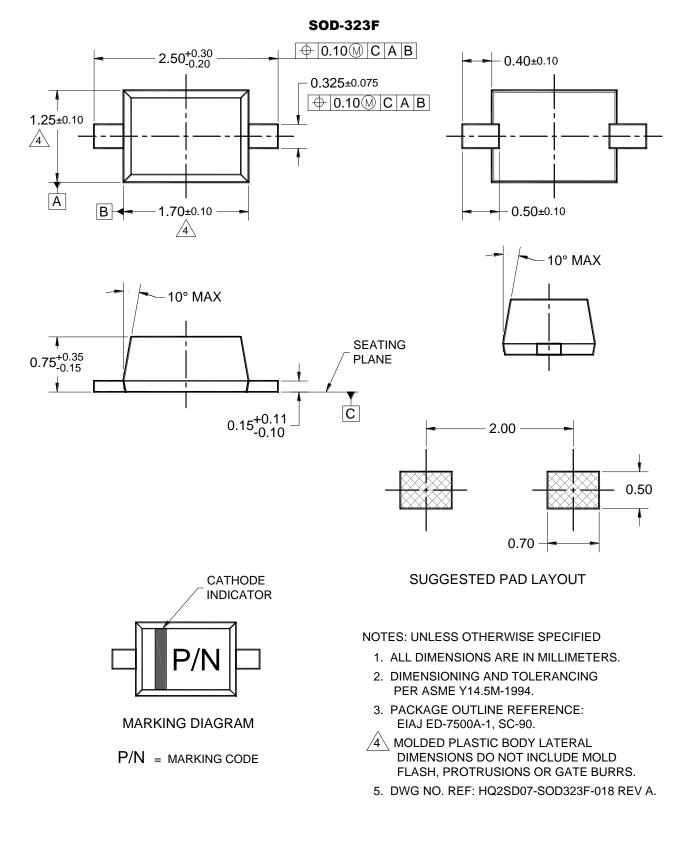


Fig.4 Power Dissipation Curve





PACKAGE OUTLINE DIMENSIONS





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