200mW, Dual PNP Small Signal Transistor

FEATURES

- AEC-Q101 qualified
- General-purpose transistors
- Ideal for automated placement
- Moisture sensitivity level: level 1, per J-STD-020
- RoHS Compliant
- Halogen-free

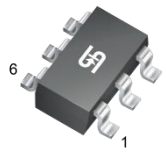
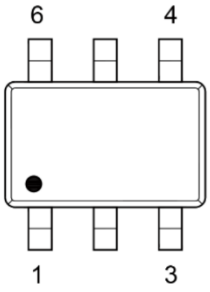
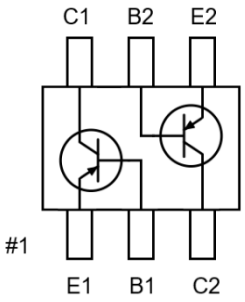
APPLICATIONS

- General switching and amplification

KEY PARAMETERS		
PARAMETER	**VALUE**	**UNIT**
V_{CBO}	-80	V
V_{CEO}	-65	V
V_{EBO}	-5	V
I_C	-100	mA
h_{FE}	450	
Configuration	Dual die	

MECHANICAL DATA

- Case: SOT-363
- Molding compound meets UL 94V-0 flammability rating
- Terminal: Matte tin plated leads, solderable per J-STD-002
- Meet JESD 201 class 2 whisker test
- Weight: 6.99mg (approximately)

PACKAGE: SOT-363	PIN CONFIGURATION	CIRCUIT DIAGRAM
		

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETER	SYMBOL	VALUE	UNIT
Power dissipation(1)	P_D	200	mW
Collector-base voltage	V_{CBO}	-80	V
Collector-emitter voltage	V_{CEO}	-65	V
Emitter-base voltage	V_{EBO}	-5	V
Collector current	I_C	-100	mA
Junction temperature	T_J	-55 to +150	°C
Storage temperature	T_{STG}	-55 to +150	°C

Note:

1. Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint

THERMAL PERFORMANCE

PARAMETER	SYMBOL	TYP	UNIT
Junction-to-ambient thermal resistance(1)	$R_{\Theta JA}$	625	°C/W

Thermal Performance Note:

1. Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint

ELECTRICAL SPECIFICATIONS (T_A = 25°C unless otherwise noted)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Collector-base breakdown voltage	I_C = -10μA, I_E = 0A	$V_{(BR)CBO}$	-80	-	-	V
Collector-emitter breakdown voltage	I_C = -10mA, I_B = 0A	$V_{(BR)CEO}$	-65	-	-	V
Emitter-base breakdown voltage	I_E = -10μA, I_C = 0A	$V_{(BR)EBO}$	-5	-	-	V
Collector-base cut-off current	V_{CB} = -30V, I_E = 0A	I_{CBO}	-	-	-15	nA
Emitter-base cut-off current	V_{EB} = -5V, I_C = 0A	I_{EBO}	-	-	-0.1	μA
DC current gain	V_{CE} = -5V, I_C = -2mA	h_{FE}	200	-	450	-
Collector-emitter saturation voltage	I_C = -10mA, I_B = -0.5mA	$V_{CE(sat)}$	-	-	-0.1	V
	I_C = -100mA, I_B = -5mA		-	-	-0.3	
Base-emitter saturation voltage	I_C = -10mA, I_B = -0.5mA	$V_{BE(sat)}$	-	-750	-850	mV
Base-emitter voltage	V_{CE} = -5V, I_C = -2mA	V_{BE}	-	-	-750	mV
Transition frequency	V_{CE} = -5V, I_C = -10mA, f = 100MHz	f_T	100	-	-	MHz
Output capacitance	V_{CB} = -10V, I_E = 0A, f = 1MHz	C_{obo}	-	-	4.5	pF

ORDERING AND MARKING INFORMATION

ORDERING CODE	PACKAGE	PACKING
BC856BSH RFG	SOT-363	3,000 / 7" Tape & Reel

CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

Fig.1 Power Dissipation Curve

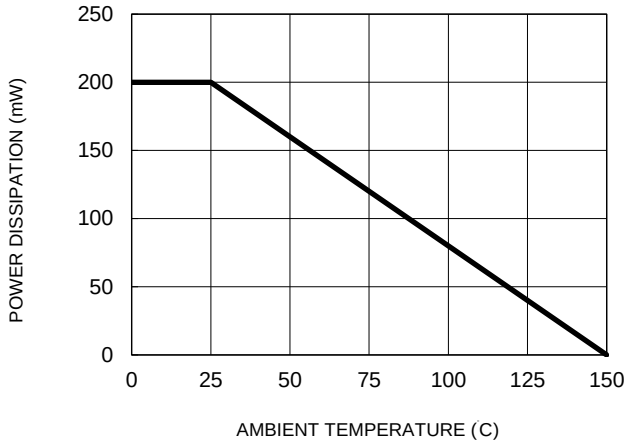


Fig.2 Typical Capacitance Characteristics

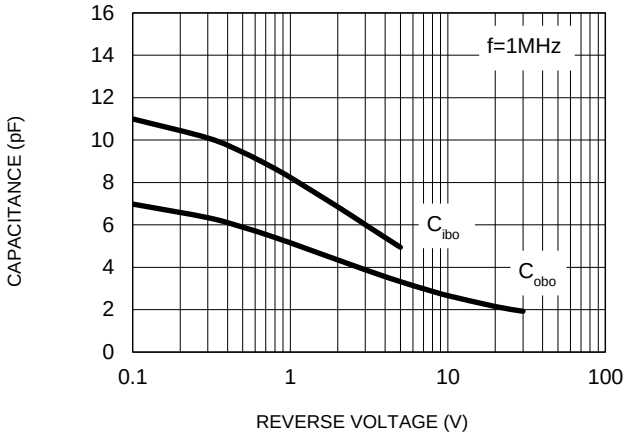


Fig.3 DC Current Gain vs. Collector Current

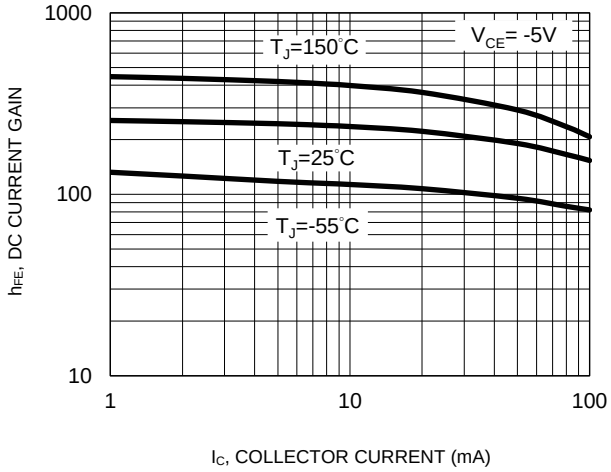


Fig.4 Collector-Emitter Saturation Voltage vs. Collector Current

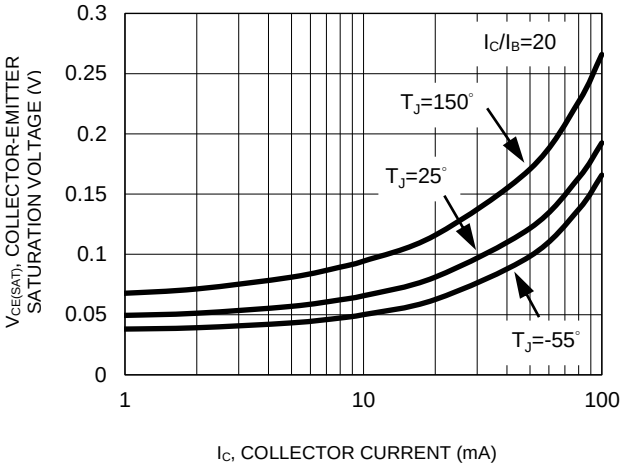


Fig.5 Base-Emitter Saturation Voltage vs. Collector Current

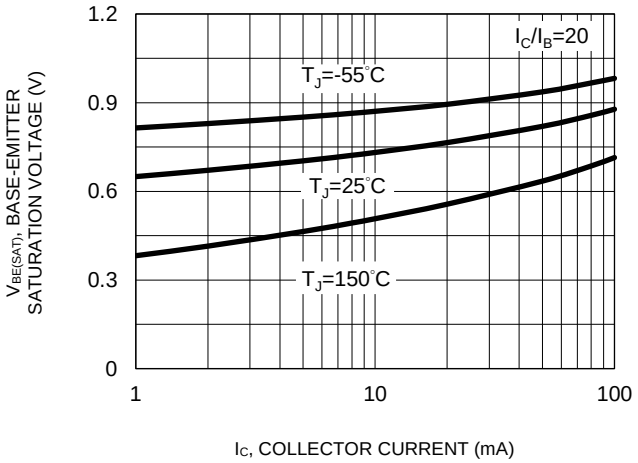
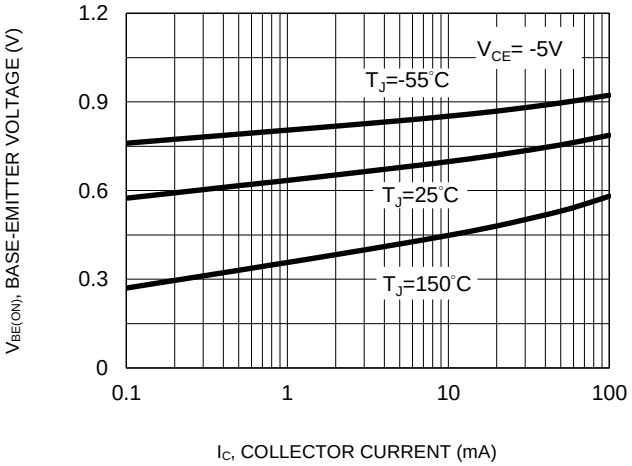
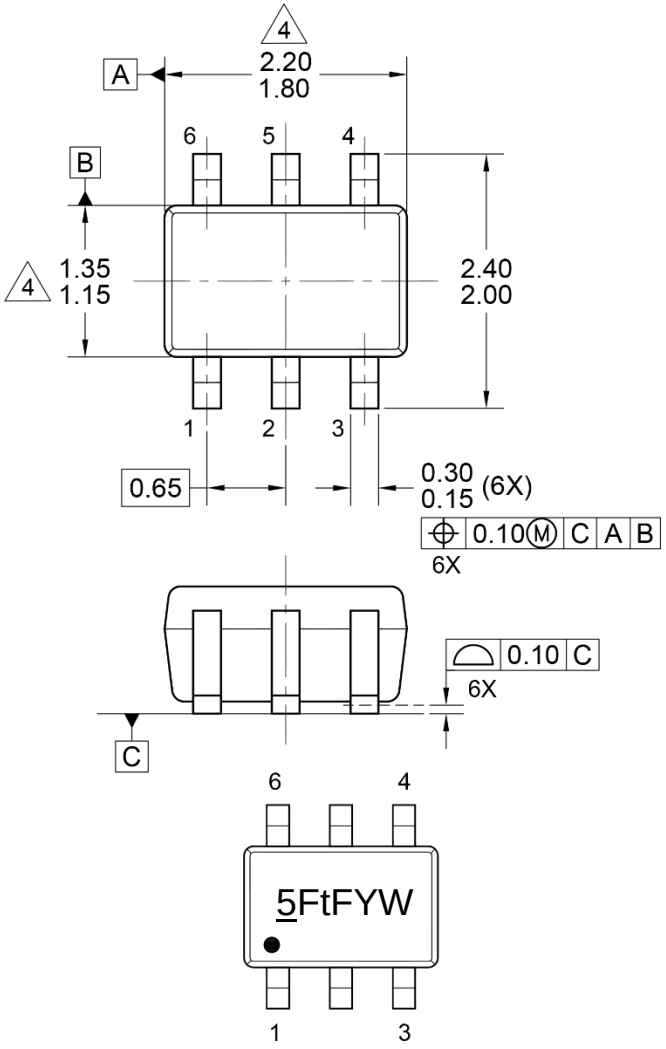


Fig.6 Base-Emitter Voltage vs. Collector Current



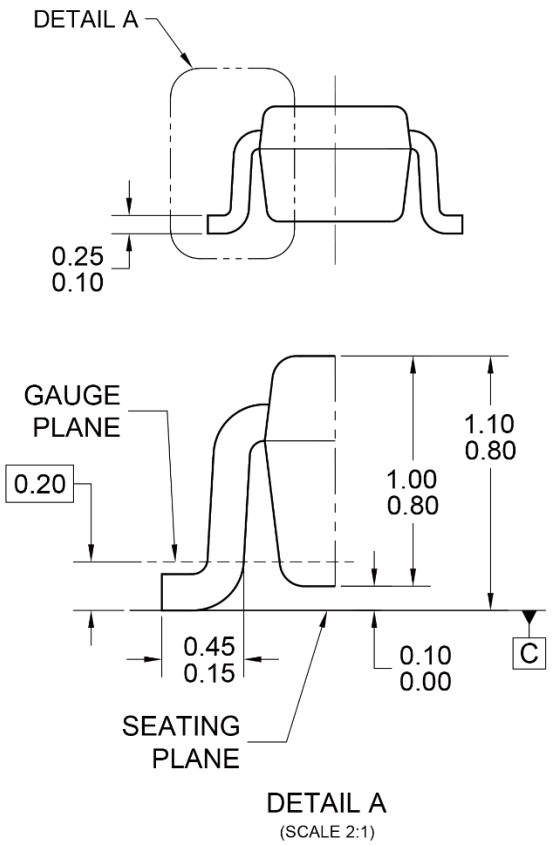
PACKAGE OUTLINE DIMENSIONS

SOT-363



MARKING DIAGRAM

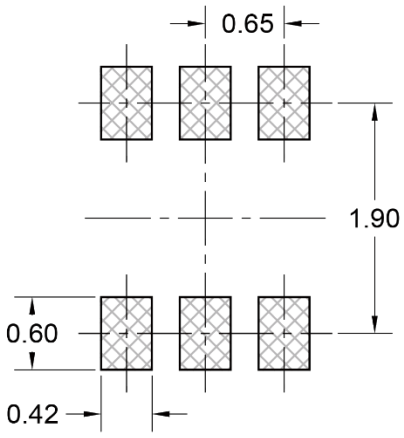
5Ft	= Device marking
F	= Factory code
Y	= Year code
W	= Bi-Week code (A~Z)



DETAIL A
(SCALE 2:1)

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PACKAGE OUTLINE REFERENCE: JEITA ED-7500A, EIAJ SC-88.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
5. DWG NO. REF: HQ2SD07-SOT363-097 REV B.



SUGGESTED PAD LAYOUT

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